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APPLICATION NOTE 3488

EEPROM Programming Instructions for DS33Z11/DS33Z44

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Abstract: The Maxim Ethernet link transport engine (ELITE) product line was created to bridge WAN to LAN. The ELITE products can be configured in several ways, the most common of which is through microprocessor (µP) control. However, for reduced-cost designs, the products can be configured using hardware pins or through an external EEPROM. While the hardware pins offers only limited functionality, the EEPROM configuration allows the user to program each register in the device. This application note was created to help the system designer properly program an EEPROM for use with the DS33Z11 or DS33Z44.

SPI Serial EEPROM Interface

The SPI interface is a four-signal serial interface that allows configuration of the DS33Z11/DS33Z44 through an external serial EEPROM. When the mode-control pins are set properly (HWMODE = 0, MODEC1 = 1, and MODEC0 = 0), the DS33Z11/DS33Z44 acts as an SPI master and reads the data from the serial EEPROM. The MOSI (master out, slave in) and MISO (master in, slave out) are for data flow, while the SPICK and active-low SPI_CS signals control access to the EEPROM. The CKPHA pin can be used to configure the sampling and update edges of the MISO and MOSI signals. The MOSI data can be output on the rising or falling edge of SPICK. The MISO data can be sampled on rising or falling edge of SPICK. The SPICK operates at a frequency of 8.33MHz, which is generated by dividing down the external 100MHz SYSCLKI signal.

SPI EEPROM Programming Sequence

Because the DS33Z11/DS33Z44 uses a fixed SPI memory-read instruction, the EEPROM used in conjunction with the DS33Z11/DS33Z44 must be a 16kB (2048 x 8) SPI serial EEPROM. SPI serial EEPROMs that have smaller memory sizes use a different memory-read instruction that is incompatible. The reading sequence begins after the initial power-on reset or the rising edge of the active-low RST pin. The DS33Z11/DS33Z44 initiates a memory read by bringing the active-low SPI_CS signal low, and then clocking out the SPI data-read instruction 0b00000011 on the MOSI data line. This is followed up by the 16-bit binary address for location 0x0000. The data is then read sequentially on the MISO data line. The active-low SPI_CS remains low until all of the data is read and latched by the DS33Z11/DS33Z44. The length of data read from the EEPROM will depend on whether the DS33Z11 or DS33Z44 is connected to the EEPROM. **Figure 1** shows the functional timing of the DS33Z11/DS33Z44 reading from the EEPROM. **Table 1** provides the memory map for the DS33Z11, while **Table 2** provides the memory map for the DS33Z44.

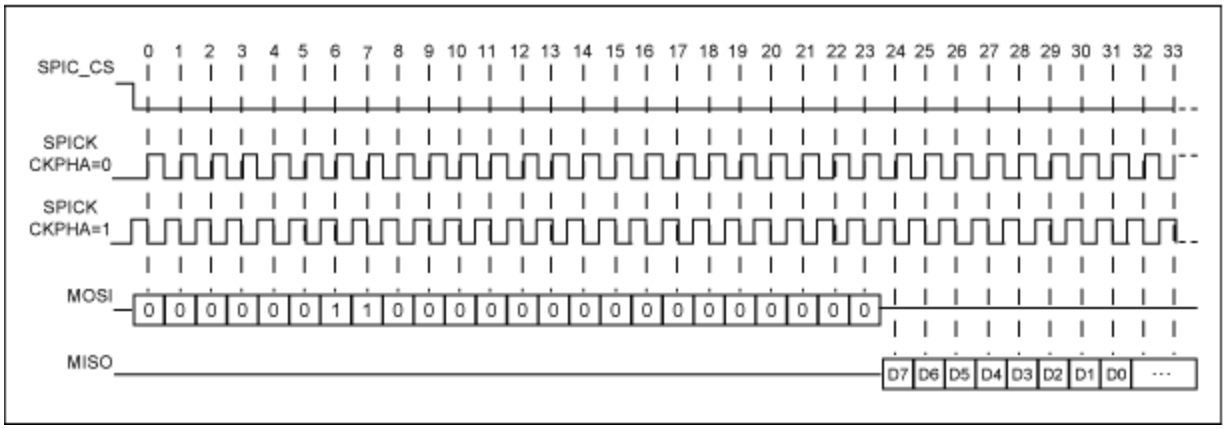

Figure 1. SPI master functional timing.

Table 1. DS33Z11 EEPROM Program Memory Map

Functional Block Address	Address Range for EEPROM Data (Hexadecimal)
Global registers	000 to 03F
Arbiter registers	040 to 07F
BERT registers	080 to 0BF
Serial interface Tx registers	0C0 to 0FF
Serial interface Rx registers	100 to 13F
Ethernet interface registers	140 to 17F
MAC register write 1 (MAC control)	180 to 186 (7-byte record for MAC indirect write)
MAC register write 2 (MII data)	187 to 18D (7-byte record for MAC indirect write)
MAC register write 3 (MII address)	18E to 194 (7-byte record for MAC indirect write)
MAC register write 4 (flow control)	195 to 19B (7-byte record for MAC indirect write)

Table 2. DS33Z44 EEPROM Program Memory Map

Functional Block Address	Address Range for EEPROM Data (Hexadecimal)
Global registers	000 to 03F
Arbiter registers	040 to 07F
BERT registers	080 to 0BF
Serial interface 1 Tx registers	0C0 to 0FF
Serial interface 1 Rx registers	100 to 13F
Ethernet interface 1 registers	140 to 17F
Serial interface 2 Tx registers	180 to 1BF
Serial interface 2 Rx registers	1C0 to 1FF
Ethernet interface 2 registers	200 to 23F
Serial interface 3 Tx registers	240 to 27F
Serial interface 3 Rx registers	280 to 2BF
Ethernet interface 3 registers	2C0 to 2FF
Serial interface 4 Tx registers	300 to 33F
Serial interface 4 Rx registers	340 to 37F
Ethernet interface 4 registers	380 to 3BF
MAC 1 register write 1 (MAC control)	3C0 to 3C6 (7-byte record for MAC indirect write)
MAC 1 register write 2 (MII data)	3C7 to 3CD (7-byte record for MAC indirect write)
MAC 1 register write 3 (MII address)	3CE to 3D4 (7-byte record for MAC indirect write)
MAC 1 register write 4 (flow control)	3D5 to 3DB (7-byte record for MAC indirect write)
MAC 2 register write 1 (MAC control)	3DC to 3E2 (7-byte record for MAC indirect write)
MAC 2 register write 4 (flow control)	3E3 to 3E9 (7-byte record for MAC indirect write)
MAC 3 register write 1 (MAC control)	3EA to 3F0 (7-byte record for MAC indirect write)
MAC 3 register write 4 (flow control)	3F1 to 3F6 (7-byte record for MAC indirect write)
MAC 4 register write 1 (MAC control)	3F7 to 3FD (7-byte record for MAC indirect write)
MAC 4 register write 4 (flow control)	3FE to 404 (7-byte record for MAC indirect write)

The Ethernet MAC specific registers are addressed indirectly and require multiple write instructions when configured using a µP in parallel port mode. Because it is not possible to directly map these indirect registers into the EEPROM memory, a special programming sequence is required when using the SPI serial EEPROM programming mode. The indirect MAC registers are programmed using separate 7-byte

records located at the end of the EEPROM memory map. Four MAC registers can be programmed in EEPROM mode: SU.MACCR, SU.MACMIID, SU.MACMIIA, and SU.MACFCR. The remaining indirect MAC registers should not need to be programmed, as they are MAC-status or status-configuration registers that require no initialization.

The 7-byte records essentially emulate the µP write sequence needed when accessing the indirect MAC registers. The first four bytes in the record contain the 32-bit data that will be written to the Ethernet MAC data 0 through 3 registers (SU.MACWD0-SU.MACWD3). The next two bytes in the record contain the 16-bit address that will be written to the Ethernet MAC address low and high registers (SU.MACAWL - SU.MACAWH). Finally, the remaining byte will be written to the Ethernet MAC read/write command status register (SU.MACRWC), which will trigger the actual write of the data to the specified address. One difference in the number of indirect writes allowed is seen in the DS33Z44. Ethernet interface 1 of the DS33Z44 has four records available for indirect writes, just like the DS33Z11. However, the remaining three Ethernet interfaces are only allowed two records for indirect writes. The reason for this is that there is only one MDIO port to manage external PHY(s), and it is controlled through MAC 1. Thus, the SU.MACMIID and SU.MACMIIA writes are only valid from the MAC 1 register set. To control more than one external PHY through the MDIO port of MAC 1, all of the PHYs MDIO ports must be tied togther and configured with the same external address.

An example is shown in **Table 3**, where the value 0x1018000C is written to the Ethernet MAC control register (SU.MACCR), which has an indirect address of 0x0000. For further assistance with the DS33Z11/DS33Z44 using the SPI serial EEPROM-programming mode, please use the links found in the following References section.

Table 3. Example of a DS33Z11 Indirect write

EEPROM 7-Byte Record	EEPROM Address Base from Table 1 (Hexadecimal)	EEPROM Address (Hexadecimal)	MAC Register Write 1 Used to Initialize SU.MACCR (Hexadecimal)
MAC data byte 1	Base + 00	180	0C - written to SU.MACWD0
MAC data byte 2	Base + 01	181	00 - written to SU.MACWD1
MAC data byte 3	Base + 02	182	18 - written to SU.MACWD2
MAC data byte 4	Base + 03	183	10 - written to SU.MACWD3
MAC address low	Base + 04	184	00 - written to SU.MACAWL
MAC address high	Base + 05	185	00 - written to SU.MACAWH
MAC write command	Base + 06	186	01 - written to SU.MACRWC

References

For further questions on the LAN-to-WAN bridge design, please contact the Telecommunication Applications support team.

For more information about the DS33Z11 or DS33Z44, please consult the appropriate data sheet available at www.maximintegrated.com/telecom.

Related Parts		
DS33Z11	Ethernet Mapper	Free Samples
DS33Z44	Quad Ethernet Mapper	Free Samples

More Information
For Technical Support: http://www.maximintegrated.com/support
For Samples: http://www.maximintegrated.com/samples
Other Questions and Comments: http://www.maximintegrated.com/contact

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