Keywords: exposed pad, exposed-pad, EP, power dissipation, TDFN, TQFN, QFN, TSSOP, TDFN, TQFN, TQFP, µMAX, µSOP, QSOP, QFN, QFND, LQFP, SOIC(N), TSSOP HYBRID

APPLICATION NOTE 3273

EXPOSED PADS: A BRIEF INTRODUCTION

Abstract: Many ICs have exposed pad packages to increase the maximum power dissipation. The stated power dissipation for packages with exposed pads always assumes the exposed pad is soldered to the PCB. This application note provides guidance on the benefits and proper user of the exposed pad.

Definition

An exposed pad is an exposed metal plate on an IC package. This application note describes pads that are located on the bottom of the package.

The exposed pad is plated with the same metal or metal alloy as the leads of the IC, usually tin.

The following is a partial list of package types that offer exposed pads as a standard or an optional configuration. New package types are always in development.

- TDFN
- TQFN
- QFN
- TSSOP
- TDFN
- TQFN
- TQFP
- µMAX
- µSOP
- QSOP
- QFN
- QFND
- LQFP
- TSSOP HYBRID
- SOIC(N)

Thermal Characteristics

Exposed pads are most often employed increase the maximum power dissipation of a package. The junction-to-case resistance (θJC) listed in the data sheet of a device with an exposed pad assumes the exposed pad is soldered or thermally bonded to a PCB, unless otherwise noted.

The data sheet for a device with an exposed pad will provide instruction as to the voltage to which the exposed pad should be connected. In most applications, the exposed pad is connected to ground, but take care to verify this on every device. A blind assumption here can provide a low-impedance short that can take many hours to analyze and a PCB revision to correct.

The pad's dimensions come from the package drawing. Some exposed pad packages have variants with different-sized exposed pads. If the data sheet is not explicit as to which variant is used, contact Technical Support to obtain further information. Create the PCB footprint with information from IPC to ensure proper allowances for both IC package tolerance and process variance.

Land Pattern Considerations for Exposed Pads

In addition to the IPC information, here are some general guidelines for creating the exposed pad's land pattern:

- The pad's land pattern must be the correct size identified in the package drawing. The exposed pad can be connected to a larger plane for increased thermal dissipation, but the pad itself must be the correct size to ensure proper soldering of the IC.
- Refer to the IC data sheet for instructions concerning the electrical potential for the exposed pad. Some pads must be connected to the ground plane, some must be electrically disconnected, and some accommodate both options.
- If the exposed pad is intended to provide significant power dissipation, the PCB designer should add vias from the exposed pad's land area to a copper polygon on the other side of the PCB. This lowers the thermal impedance from the IC to the ambient air.
- Hand assembling PCBs with electrically connected exposed pads is highly discouraged. The only practical way to achieve this is to include a single large via in the center of the land to allow the application of a soldering iron to the bottom of the IC through this hole. The best approach is to use a standard SMT assembly process with carefully controlled parameters to ensure reliable and repeatable results.

More Information
For Technical Support: https://www.maximintegrated.com/en/support
For Samples: https://www.maximintegrated.com/en/samples
Other Questions and Comments: https://www.maximintegrated.com/en/contact

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