

Design Note:

**HFDN-31.0**

Rev.1; 04/08

---

---

**MAX3610 Synthesizer-Based Crystal Oscillator  
Enables Low-Cost, High-Performance Clock Sources**

---

---

# MAX3610 Synthesizer-Based Crystal Oscillator Enables Low-Cost, High-Performance Clock Sources

## 1 Introduction

The MAX3610 is a synthesizer-based crystal oscillator IC optimized for use in Fiber Channel (FC) storage area network applications, such as Hard Disk Drive, Host Bus Adapter, Switch and RAID Controller. The device incorporates a fully-integrated crystal oscillator and a frequency multiplier based on a phase locked loop (PLL). Using a low-cost 26.5625MHz AT-cut fundamental crystal resonator, the device generates a 106.25MHz or 212.5MHz clock output with either an LVPECL or an LVDS interface. The output clock phase jitter is typically  $0.7\text{ps}_{\text{rms}}$  in a bandwidth of 12kHz to 20MHz.

This design note describes the characteristics of the MAX3610 reference clock generator, and the methodology for measuring the power supply induced deterministic jitter using a spectrum analyzer. Measurement results are presented for the clock output single-side-band (SSB) phase noise and the power supply induced deterministic jitter. The recommended crystal resonator parameters and the measured frequency stability of the MAX3610 with a crystal are given in Section 4 of this document.

## 2 Crystal Oscillator with PLL Synthesizer

Traditional 1Gbps and 2Gbps FC applications use a 106.25MHz crystal-based oscillator with single-ended LVCMOS interface as a reference clock source. As the FC serial data rate is moving towards 4.25Gbps today and probably 8.5Gbps in the next generation, system designers tend to use higher reference clock frequencies, such as 212.5MHz with a differential LVPECL or LVDS interface, to meet the jitter requirement of the application. To achieve such a high frequency, the traditional 3<sup>rd</sup> overtone or 5<sup>th</sup> overtone crystal oscillator becomes more expensive due to high crystal manufacturing costs.

The MAX3610 provides a low-cost clock module solution by using a fundamental AT-cut crystal resonator to generate a high-frequency, low-jitter clock output. The functional block diagram is shown in Figure. 1.

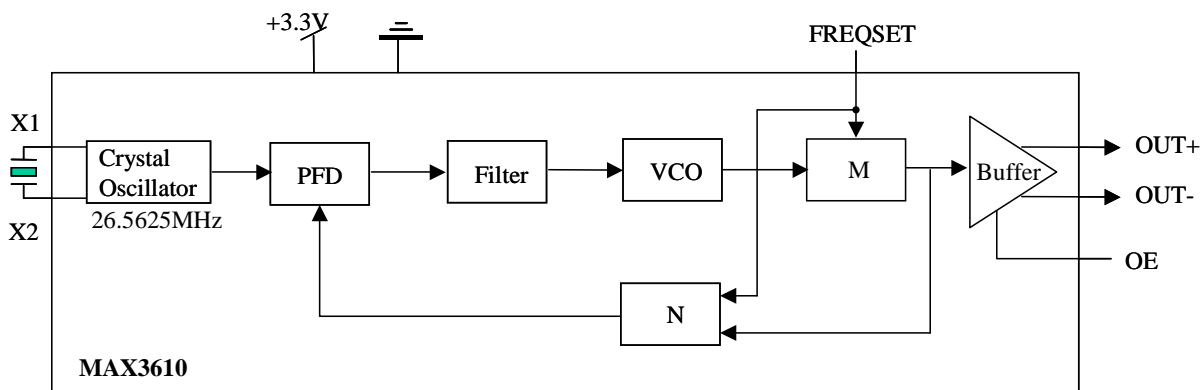


Figure 1. Synthesizer-based Crystal Oscillator

With the crystal oscillation frequency  $f_{xo}$  running at 26.5625MHz, the MAX3610 output frequency  $f_{out}$  is given by:

$$f_{out} = f_{osc} \times N \quad (1)$$

N is the frequency multiplication factor, controlled by the external FREQSET pin. The control setting is given in Table I:

**Table 1. Output clock frequency control setting:**

FREQSET	N	Output Frequency
VCC or open	4	106.25MHz
GND	8	212.5MHz

To optimize the SSB phase noise at the clock output, considerable care has been taken in designing the MAX3610 PLL and VCO. The clock output phase noise is determined by the low-frequency crystal

oscillator phase noise,  $\Phi_{XO}(f)$ , the VCO phase noise,  $\Phi_{VCO}(f)$ , and the PLL voltage noise,  $V_N(f)$ , from the phase detector and loop filter. The PLL phase model is illustrated in Figure 2, where  $K_d$  is the phase detector gain,  $F(s)$  is the loop filter transfer function, and  $K_o$  is the on-chip VCO frequency control sensitivity.

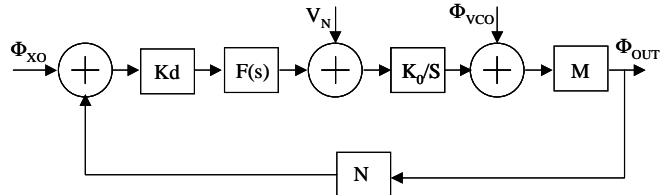


Figure 2. MAX3610 PLL Phase Model

By trading-off the noise contributions from  $\Phi_{XO}(f)$ ,  $V_N(f)$  and  $\Phi_{VCO}(f)$ , the MAX3610 PLL 3dB bandwidth is set at approximately 50kHz. The measured output SSB phase noise at 106.25MHz is shown in Figure 3. The calculated phase jitter is 0.7ps-rms when the phase noise is integrated from 12kHz to 20MHz.

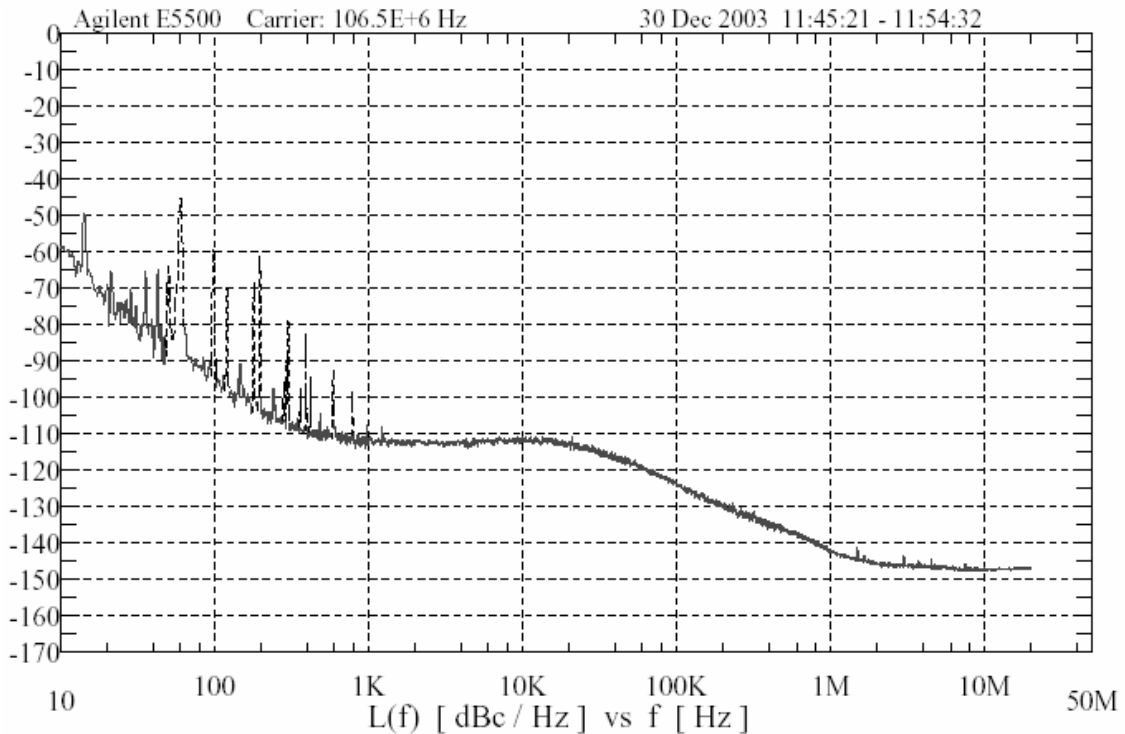


Figure 3. MAX3610 Output SSB phase noise at 106.25MHz(LVDS)

### 3 Power Supply Noise Rejection

In a real system, power supply noise comes from different sources: random noise, digital spikes from switch supply or other digital circuits. Even with good supply filtering, there is still some noise on the supply which, when injected into the active components on board, may degrade the signal quality.

Special considerations have been taken for the MAX3610 crystal oscillator gain block, PLL and VCO design to achieve good power supply noise rejection.

To characterize the power supply noise rejection for a clock source, a sinusoidal signal is injected into the power supply, and the deterministic jitter is measured at each single frequency tone. There are different kinds of equipment that can be used to perform this measurement, for example an oscilloscope, a time interval analyzer (TIA), or a spectrum analyzer. If the amount of deterministic jitter is large enough, a bimodal distribution can be observed from the oscilloscope histogram, and the deterministic jitter can be measured at the time offset of T/2 from the trigger point, where T is the period of the modulation signal.

A spectrum analyzer is used to accurately measure the MAX3610 clock output deterministic jitter. The measurement setup is shown in Figure 4.

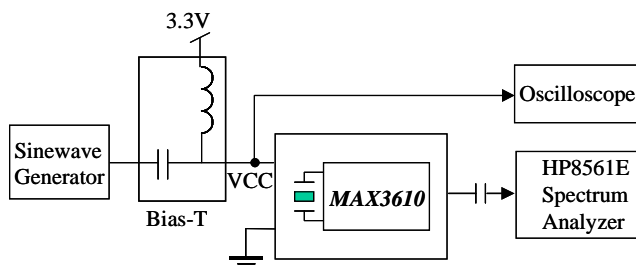


Figure 4. Measurement setup for supply-induced deterministic jitter

The sinusoidal tone on the supply produces a frequency modulated output clock with a reduced modulation index  $\Delta f/f_m$ , where  $\Delta f$  is the frequency deviation caused by the supply modulation signal having a frequency  $f_m$ . For a small modulation index, the spectrum consists mainly of the carrier and two sideband signals sited  $\pm f_m$  around the carrier. The magnitude of the two sideband spectral lines relative to the carrier is dependent upon the modulation index. This in turn affects the maximum phase deviation perceived here as deterministic jitter. This deterministic jitter is given by:

$$DJ(ps_{p-p}) = \frac{2 \times 10^{x(\text{dBc})/20}}{\pi \times f_{out}} \quad (2)$$

$x$  is the sideband frequency modulation magnitude relative to the carrier magnitude. Figure 5 shows the deterministic jitter in  $UI_{p-p}$  versus  $x$  in dBc.

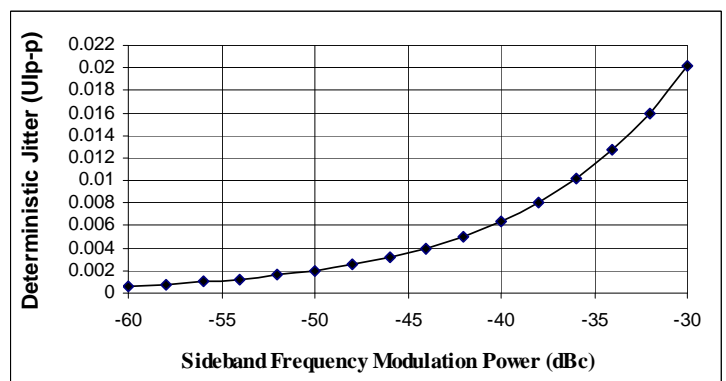


Figure 5. Deterministic jitter caused by single tone frequency modulation

As an example, if a 100kHz sinusoidal signal is injected into the power supply, and the measured frequency modulation spectral line at  $(f_{out} \pm 100kHz)$  is -50dBc relative to the carrier frequency  $f_{out}$ , then according to Figure 5, the deterministic jitter is  $2mUI_{p-p}$ . This corresponds to  $18.8ps_{p-p}$  if the carrier frequency is 106.25MHz.

As another example, a sinusoidal signal with amplitude of 50mV is injected into the supply, and its frequency is swept from 5kHz to 1MHz. The measured MAX3610 supply induced deterministic jitter can be seen in Figure 6.

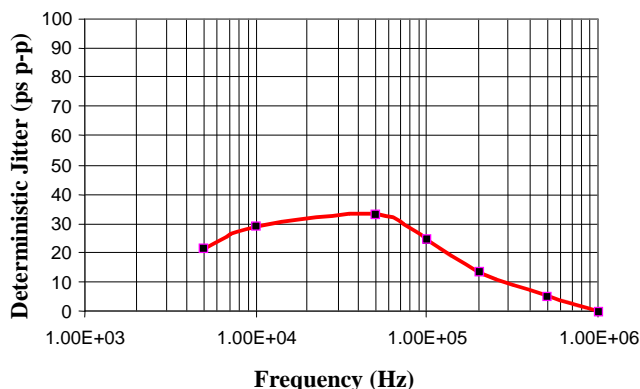


Figure 6. MAX3610 supply-induced deterministic jitter

## 4 Crystal Resonator Selection:

Figure 7 shows the crystal model and the crystal connection to MAX3610. The recommended crystal resonator parameters can be found in table II.

Table 2. Crystal Parameters

Parameter	Value
Crystal	Fundamental AT cut
Nominal Oscillator Frequency	26.5625MHz
Shunt Capacitance (Co)	2pF
Co/Cs	280
Load capacitance	12pF
Equivalent Series Resistance (ESR)	5Ω to 40Ω

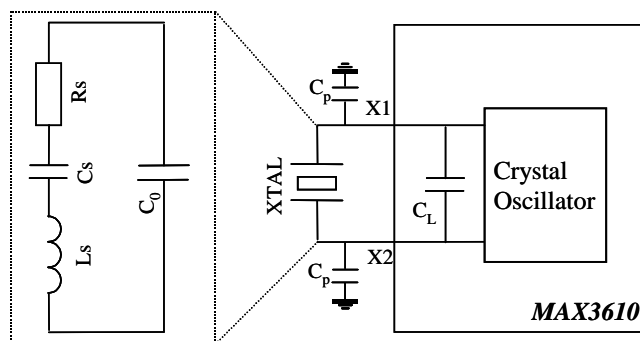


Figure 7. Crystal model and crystal connection to MAX3610

The crystal total load capacitance includes the MAX3610 oscillation circuit input capacitance  $C_L$  as well as the parasitic capacitance  $C_p$  caused from the assembling/packaging of the blank crystal and the IC. It is important to place the crystal as close as possible to the MAX3610 to minimize the parasitic capacitance  $C_p$ , so that the total load capacitance is dominated by the MAX3610 on-chip capacitor  $C_L$ .

The crystal series resonant frequency  $f_s$  and its relation to the crystal oscillator frequency  $f_{xo}$  is given below:

$$f_{xo} = f_s \times \left(1 + \frac{C_s}{2(C_o + C_L)}\right) \quad (3)$$

and

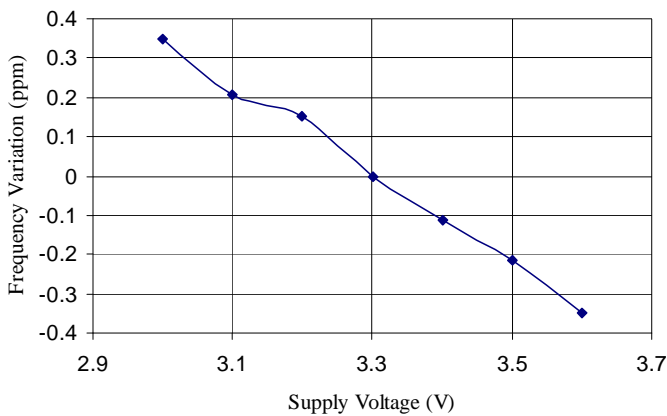
$$f_s = \frac{1}{2\pi\sqrt{L_s \times C_s}} \quad (4)$$

From the equation (3), we can estimate that the frequency shift due to load capacitance variation is about 20ppm/pF. The MAX3610 input capacitance  $C_L$  is trimmed within  $\pm 10\%$  of the nominal value.

## 5 Frequency Stability

When a clock module is built using the MAX3610 die and a crystal resonator, the output clock frequency stability over temperature will be determined by the crystal temperature coefficient, as well as the load capacitor variation over temperature. The MAX3610 input capacitance variation from 0°C to 85°C is controlled well within 1%, which results in less than 2ppm variation over the entire temperature range. Therefore, the clock output frequency stability is mainly determined by the crystal temperature characteristics.

The MAX3610 crystal oscillator gain block characteristics have little dependence on the supply variation. Figure 8 shows that the frequency varies less than 1ppm when supply voltage is changed from 3.0V to 3.6V.



*Figure 8. MAX3610 frequency variation over supply*

In addition, the MAX3610 crystal oscillation gain block has the automatic amplitude control which maintains an almost constant AC power, consistent with the power levels required for reduced crystal aging.

## 6 Conclusion

The MAX3610 provides a low cost solution for high frequency and high performance clock modules. To obtain MAX3610 die samples, or for information regarding the use of the MAX3610 for other frequencies or other applications, please contact your local Maxim sales representative.