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APPLICATION NOTE 1805

Choosing the MAX1932 External Inductor, Diode, Current-Sense Resistor, and Output Filter Capacitors for Worst-Case Conditions

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The MAX1932 is a boost converter controller targeted for avalanche photodiode (APD) bias supplies in medium to long reach optical communication networks. Although the MAX1932 can operate in either continuous or discontinuous conduction mode, due to the high ratio of output voltage to input voltage for an APD bias application and high-switching frequency, discontinuous conduction mode boost topology is chosen. This application note describes the fixed-frequency discontinuous conduction mode boost topology and shows how to select the inductor, diode, and output filter capacitors for worst-case conditions.

Discontinuous mode means that there is an interval during a switching cycle where the inductor current is zero. Refer to the schematic of **Figure 1** and the associated waveforms of **Figure 2**. At the beginning of each switching cycle, the MOSFET (Q1) turns on, thus applying the input voltage across the inductor (L1). The inductor current ramps up from zero to a peak value (I_{L1_PK}) required to store enough energy to support the output. This stored energy will be completely released to the output via diode D1 prior to the end of Q1 off time, where the inductor current decays to zero.

The energy stored and released by the inductor L1 every switching cycle is:

$$E_S = 0.5L1 \times (I_{L1\_PK})^2 \qquad \text{(Eq. 1)}$$

At the switching frequency, f_S, the power released from the inductor is then:

$$P_{L1} = E_S \times f_S = 0.5L1 \times (I_{L1\_PK})^2 \times f_S \qquad \text{(Eq. 2)}$$

This power is equal to the maximum output power plus any power losses in the circuit.

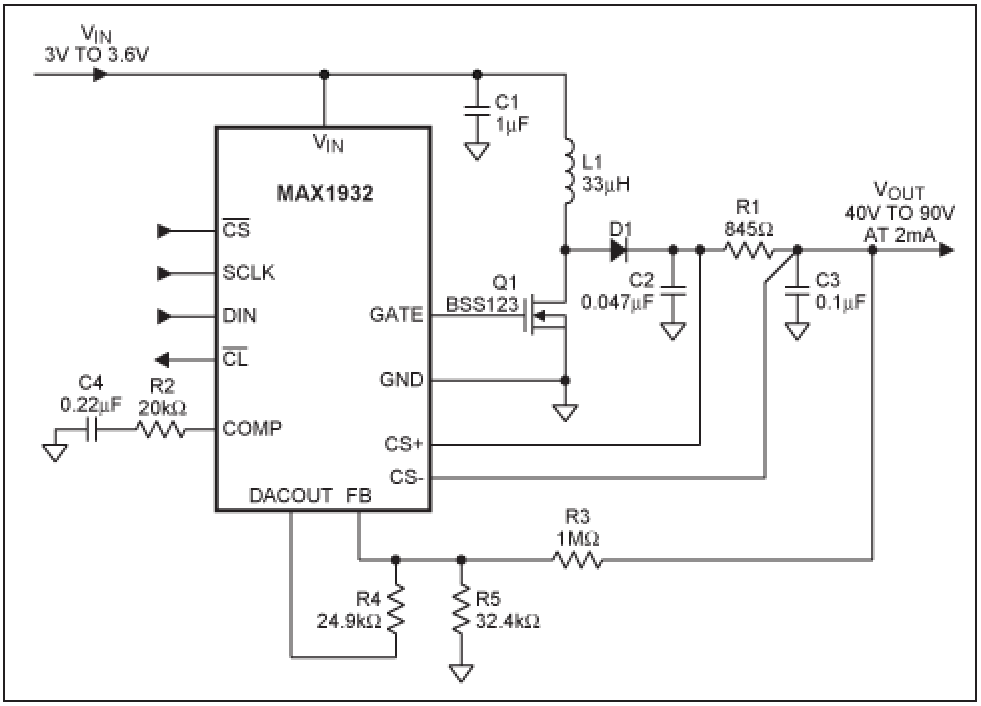

Figure 1. Typical application circuit for 3V to 3.6V input, 40V to 90V output at 2mA.

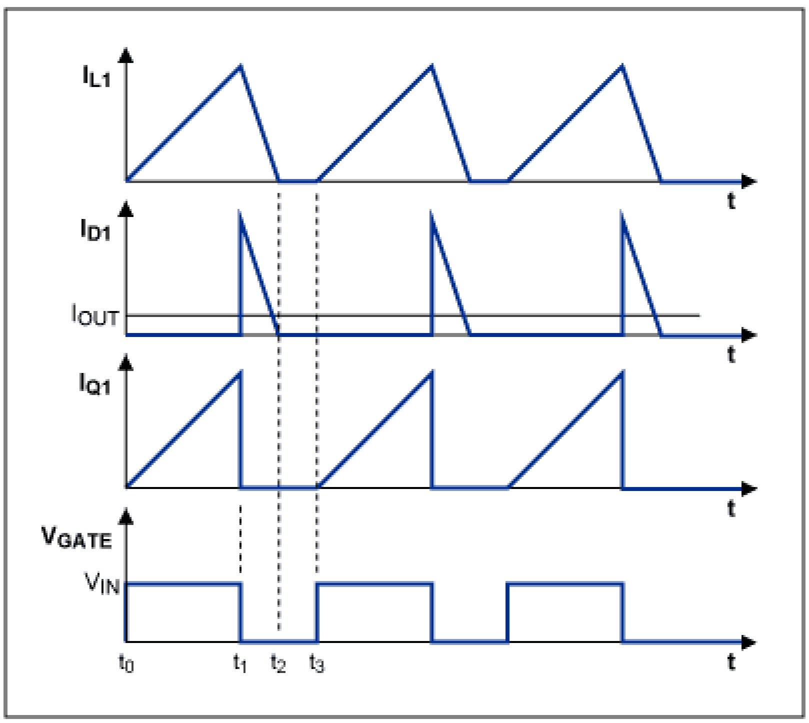

Figure 2. Waveforms of inductor current (I_{L1}), diode current (I_{D1}), MOSFET switch current (I_{Q1}), and gate voltage (V_{GATE}).

This can be expressed by the equation below:

$$0.5L1\ (I_{L1\_PK})^2 \times f_S = P_{O\_MAX}/\eta = V_{O\_MAX} \times I_{O\_MAX})/\eta \qquad \text{(Eq. 3)}$$

Where η is the efficiency of the circuit, taken into consideration of the power losses as mentioned above.

The value of the peak inductor current is a function of the input voltage, the operating duty cycle, D, and the switching frequency:

$I_{L1\_PK} = (V_{IN} \times D)T_S/(L1)$ (Eq. 4)

Where $T_S = 1/f_S$, the switching period.

Substituting I_{L1_PK} of (4), into (3), and solve for L1:

$L1 = ((V_{IN} \times D)^2 \times T_S \times \eta)/(2 \times V_{O\_MAX} \times I_{O\_MAX})$ (Eq. 5)

To ensure that under worst-case voltage conditions and component tolerances, the value of L1 must meet the requirement below:

$L1_{MAX} = ((V_{IN\_MIN} \times D_{MAX})^2 \times T_{S\_MIN} \times \eta_{MIN})/(2 \times V_{O\_MAX} \times I_{O\_MAX})$ (Eq. 6)

Since $T_{S\_MIN} = 1/f_{S\_MAX}$, then:

$L1_{MAX} = ((V_{IN\_MIN} \times D_{MAX})^2 \times \eta_{MIN})/(2 \times V_{O\_MAX} \times I_{O\_MAX} \times f_{S\_MAX})$ (Eq. 7)

Where D_{MAX} is the maximum duty cycle at the highest switching frequency.

For the MAX1932, select D_{MAX} of 0.85 to allow about 5% margin from the data sheet typical specification. The value of η_{MIN} can be set at 0.70 as a starting point, for calculating the inductor value. Since low-cost commercial inductors can have tolerance in the range from, ±10% to ±20%, make sure that with worst-case tolerance the inductor value does not exceed $L1_{MAX}$. For example with ±10% tolerance, the nominal inductance value is then:

$L1 = L1_{MAX}/1.10$ (Eq. 8)

The calculated inductance value should be verified with test results, and a final tweak to the calculated value can be made if deemed necessary. The value calculated was based on worst case when the switching frequency is at maximum value, as specified in the MAX1932 data sheet. At any other switching frequency in the specified range, and at V_{IN_MIN}, V_{O_MAX}, I_{O_MAX} the measured operating duty cycle should not exceed $D_{MAX(fs)}$ below:

$D_{MAX(fs)} = D_{MAX(fs/fs\_MAX)}{}^{1/2} = 0.85(f_S/340kHz)^{1/2}$ (Eq. 9)

Where f_{S_MAX} is the maximum switching frequency of 340kHz, due to the tolerance of the internal oscillator of the MAX1932.

If the measured operating duty cycle is higher then $D_{MAX(fs)}$, then the efficiency η is probably lower than the 0.70 assumed as a starting point. In this case the value of the inductor needs to be lowered. If the measured duty cycle is less than $D_{MAX(fs)}$, the circuit will work under all worst-case conditions. However if it is much lower then the required $D_{MAX(fs)}$, it is undesirable, since this would result in unnecessary higher peak current that would degrade the efficiency. It is suggested to have the operating duty cycle in the range of 0.95 × D_{MAX} to D_{MAX}. To increase the operating duty cycle, raise the inductance value.

Once the inductor value is determined, the maximum peak operating steady state inductor current is:

$$I_{PK\_MAX} = V_{IN\_MIN} \times D_{MAX} \times (f_{SMIN}/f_{S\_MAX})^{1/2}/(f_{S\_MIN} \times L_{MIN}) \qquad \text{(Eq. 10)}$$

Note that under an output step load transient, the maximum peak inductor current can momentarily be higher, and the absolute maximum value is:

$$I_{PK\_TMAX} = (V_{IN\_MAX} \times D_{MAX})/(f_{S\_MIN} \times L_{MIN}) \qquad \text{(Eq. 11)}$$

Make sure that the inductor does not saturate at this maximum peak transient current.

The time required for the inductor current to ramp up from zero to I_{PK_MAX} (t1–t0 in Figure 2) is:

$$T_{RUP} = I_{PK\_MAX} \times L_{MIN}/V_{IN\_MIN} \qquad \text{(Eq. 12)}$$

The time requires to ramp down from the I_{PK_MAX} above to zero (t2–t1 in Figure 2) is:

$$T_{RDWN} = (V_{IN\_MIN} \times T_{RUP})/(V_{O\_MAX} - V_{IN\_MIN}) \qquad \text{(Eq. 13)}$$

The maximum average inductor current is:

$$I_{L1\_AVG} = 0.5 I_{PK\_MAX} \times (T_{RUP} + T_{RDWN}) \times f_{S\_MIN} \qquad \text{(Eq. 14)}$$

The inductor current flows through the MOSFET during the ramp-up interval, and through the diode, D1, during the ramp-down interval. Hence, the maximum RMS current through the FET is:

$$I_{Q1\_RMS} = I_{PK\_MAX} (T_{RUP} \times f_{SMIN}/3)^{1/2} \qquad \text{(Eq. 15)}$$

And the diode average current is:

$$I_{D1\_AVG} = 0.5 I_{PK\_MAX} \times T_{RDWN} \times f_{S\_MIN} \qquad \text{(Eq. 16)}$$

For most APD bias supply application, the average diode current is less than 5mA, therefore a small Schottky or silicon switching diode can be used. Ensure that the Q1, D1, C2 and C3 voltage rating are sufficiently higher than the maximum output voltage.

Ceramic capacitors have low equivalent series resistance (ESR) and inductance (ESL) at high frequency, with low capacitance value for small size and low cost. They are recommended for output filtering. For the circuit of Figure 1, in addition to the typical output filter capacitor, C2, there is a lowpass filter formed by R1 and C3 to further reduce the switching ripple to a very low level to bias the APD diode. The peak-to-peak ripple voltage across C2 is comprised of the ripple due to its ESR, ESL and the capacitance charge displacement. The three ripple components are additive and superimpose on each other to yield the total worst-case peak-to-peak ripple voltage at C2 of:

$$V_{C2\_RPL} = (I_{PK\_MAX} \times ESR) + (V_{O\_MAX} - V_{IN\_MIN}) \times (ESL/L1) + [I_{O\_MAX} \times ((1/f_{S\_MIN}) - T_{RDWN})/C2] \qquad \text{(Eq. 17)}$$

The resistor R1 serves two purposes, as a current-sense resistor for cycle to cycle current limit and as part of an RC lowpass filter to attenuate the switching ripple voltage. The value of R1 is chosen so that the voltage drop across R1 at maximum output current and ripple voltage does not trip the minimum current limit threshold of 1.8V. Hence R1 can be calculated as:

$$R1 = (1.8V - 0.5V_{R1\_RPL})/I_{O\_MAX} \quad \text{(Eq. 18)}$$

Where V_{R1_RPL} is the peak-to-peak ripple voltage across R1, and can be expressed as:

$$V_{R1\_RPL} = V_{C2\_RPL} [1 - (1/(2 \times \pi \times R1 \times C3 \times f_{S\_MIN}))] \quad \text{(Eq. 19)}$$

Solving for R1 from (18) and (19) yields:

$$R1 = \frac{(1.8 - 0.5V_{C2\_RPL}) + \sqrt{(1.8 - 0.5V_{C2\_RPL})^2 + \frac{I_{O\_MAX} \times V_{C2\_RPL}}{\pi \times C3 \times f_{S\_MIN}}}}{2I_{O\_MAX}} \quad \text{(Eq. 20)}$$

The worst-case output peak-to-peak ripple voltage, V_{O_RPL}, is then :

$$V_{O\_RPL} = V_{C2\_RPL}/(2 \times \pi \times R1 \times C3 \times f_{S\_MIN}) \quad \text{(Eq. 21)}$$

As seen from (21), the output ripple voltage is inversely proportional to the value of R1 and C3. However the value of R1 is bounded by the current limit circuit as shown in (20), while the value of C3 is only limited by its size and cost.

Since ceramic capacitors have very low ESR and ESL, the ripple voltage across C2 as expressed in (17) is mostly caused by the capacitor's value. Therefore, we can say that the output ripple voltage is also inversely proportional to the value of C2. Similar to C3, the value of C2 is only limited by its size and cost.

Make sure that the value of C2 and C3 are large enough to cover their tolerances and variation due to temperature.

Below is a design example using the above equations:

V_{IN}: 3V (min), 3.6V (max)
V_O: 40V (min), 90V (max)
V_{O_RIPPLE}: < 1.5mV$_{P-P}$
I_O: 2mA (max)
f_S: 250kHz (min), 340kHz (max)
C2 = 0.047µF, ESR = 5mΩ, ESL = 1nH
C3 = 0.1µF

First, select D_{MAX} = 0.85 and η_{MIN} = 0.70, calculate $L1_{MAX}$ per (7) above:

$L1_{MAX}$ = 37.19µH

For ±10% tolerance, the nominal L1 value is:

L1 = 37.19µH/1.1 = 33.8µH

Use a standard inductor value of 33µH. Hence, $L1_{MIN}$ = 0.9 × 33µH = 29.7µH

Now, calculate the worst-case maximum peak steady state and transient inductor current using (10) and (11):

I_{PK_MAX} = 294mA (peak) and I_{PK_TMAX} = 412mA (peak)

From (12), (13), and (14), the average inductor DC current is:

I_{L1_AVG} = 111mA

Note that the currents above only occur when the switching frequency and inductor are at minimum value due to tolerances. As mentioned above, select the inductor with the rated saturation current above 353mA.

From (12) and (15), the RMS current of Q1 is:

I_{Q1_RMS} = 145mA

From (13) and (16), the average current of D1 is:

I_{D1_AVG} = 3.7mA

From (17), (18), (19), and (20), the value of the current-sense and filtering resistor, R1, is:

R1 = 856.5Ω

Select 845Ω, 1%, the next standard value lower than the 856.5Ω calculated. From (17), and (21), the worst-case output peak-to-peak ripple voltage is:

V_{O_RPL} = 1.28mV_{P-P}

As previously stated, the value of C2 and C3 can be increased to further reduce the output ripple. For example, doubling the value of C2 or C3 will cut the output ripple in half.

It has been shown how to select the inductor (L1), diode (D1), current-sense resistor (R1), and filter capacitors (C2 and C3) to meet the output voltage, output current and ripple requirement for worst-case conditions that include input voltage, switching frequency variation, current-limit-threshold variation.

Related Parts		
MAX1932	Digitally Controlled, 0.5% Accurate, Safest APD Bias Supply	Free Samples

Application Note 1805: http://www.maximintegrated.com/an1805
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