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TUTORIAL 1051

SEPIC Equations and Component Ratings

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Lithium batteries, power-factor converters, and improved low-ESR capacitors are giving a new shine to the classic SEPIC topology. A SEPIC (single-ended primary inductance converter) is distinguished by the fact that its input voltage range can overlap the output voltage. Because SEPIC literature is pretty thin, however, a design engineer not expert in energy converters may feel helpless when asked to design one of these circuits.

This article provides an understanding of basic SEPIC equations, and proposes clear and simple formulas for rating the main components and predicting performance.

Lithium batteries have been very successful, thanks mostly to their impressive energy density. A single lithium cell provides an open voltage of 4.2V when fully charged, and replaces (almost) three of its NiCd or NiMH counterparts. This voltage depends somewhat on residual capacity, and the cell still retains some energy down to 2.7V. Such input voltage ranges above and below the output of many DC/DC converters, and thereby eliminates the possibility of using an exclusively step-up or step-down type of converter.

SEPICs also find application in the power supplies for power-factor converters (PFCs). Most such circuits use a simple step-up converter as the input stage, implying that the stage output must exceed the peak value of the input waveform. AC inputs of $240V_{RMS}$ ±20%, for example, impose an output of at least 407V, forcing the following converters to work with elevated input voltages. By accepting medium to low input voltages, the SEPIC topology provides a more compact and efficient design. It provides the required output level even if the peak input voltage is higher.

Basic Equations

The boost (often called step-up) topology (**Figure 1**) is the basis for the SEPIC converter. The boost-converter principle is well understood: first, switch Sw closes during T_{ON}, increasing the magnetic energy stored in inductance L1. Second, the switch opens during T_{OFF}, offering D1 and C_{OUT} as the only path for stored magnetic energy to flow. C_{OUT} filters the current pulse generated by L1 through D1. When V_{OUT} is relatively low, you can improve the efficiency by using a Schottky device with low forward voltage (about 400mV) for D1. V_{OUT} must be higher than V_{IN}. In the opposite case ($V_{IN} > V_{OUT}$) D1 is forward biased, and nothing prevents current flow from V_{IN} to V_{OUT}.

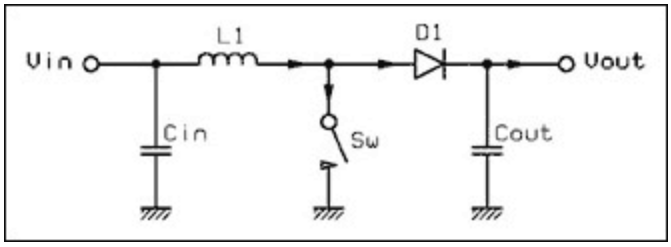

Figure 1. This boost-converter topology is the basis for SEPIC power-supply circuits.

The SEPIC scheme of **Figure 2** removes this limitation by inserting a capacitor (Cp) between L1 and D1. This capacitor obviously blocks any DC component between the input and output. D1's anode, however, must connect to a known potential. This is accomplished by connecting D1 to ground through a second inductor (L2). L2 can be separate from L1 or wound on the same core, depending on the needs of the application. Because the latter configuration is simply a transformer, one might object that a classical flyback topology is more appropriate in that case. The transformer leakage inductance, however, which is no problem in SEPIC schemes, often requires a "snubber" network in flyback schemes. The main parasitic resistances R_{L1}, R_{L2}, R_{SW}, and R_{Cp} are associated with L_1, L_2, S_W, and Cp respectively.

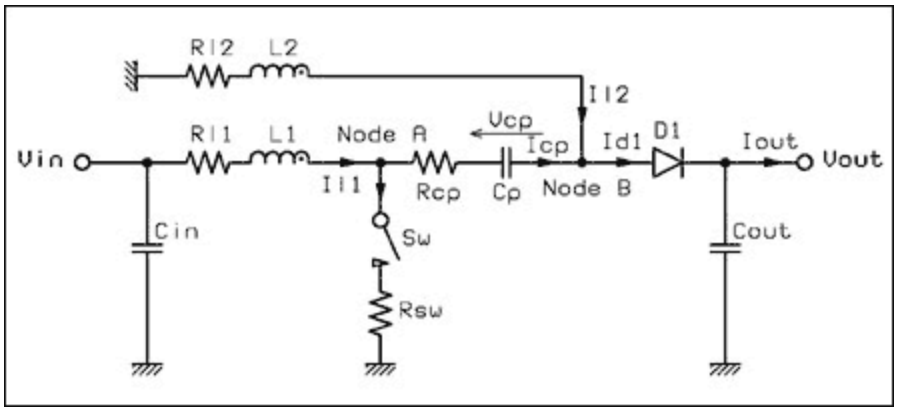

Figure 2. An advantage of the SEPIC circuit, besides buck/boost capability, is a capacitor (Cp) that prevents unwanted current flow from V_{IN} to V_{OUT}.

Though it has very few elements, the operation of a SEPIC converter is not so simple to abstract into equations. We assume that the values of current and voltage ripple are small with respect to the DC components. To start, we express the fact that at equilibrium there is no DC voltage across the two inductances L1 and L2 (neglecting the voltage drop across their parasitic resistances). Therefore, Cp sees a DC potential of V_{IN} at one side, through L1, and ground on the other side, through L2. The DC voltage across Cp is:

$(V_{Cp})_{mean} = V_{IN}$
(Eq. 1)

"T" is the period of one switching cycle. Call α the portion of T for which Sw is closed, and $1-\alpha$ the remaining part of the period. Because the mean voltage across L1 equals zero during steady-state conditions, the voltage seen by L1 during α T (Ton) is exactly compensated by the voltage seen during $(1-\alpha)$T (Toff):

$\alpha\, TV_{IN} = (1-\alpha)\, T\, (V_{OUT} + V_D + V_{Cp} - V_{IN}) = (1-\alpha)\, T\, (V_{OUT} + V_D)$.

V_D is D1's forward voltage drop for a direct current of (IL1 + IL2), and V_{Cp} is equal to V_{IN}:

$(V_{OUT} + V_D) / V_{IN} = \alpha / (1-\alpha) = Ai$
(Eq. 2)

Ai is called the amplification factor, where "i" represents the ideal case for which parasitic resistances are null. Neglecting V_D with respect to V_{OUT} (as a first approximation), we see that the ratio of V_{OUT} to V_{IN} can be greater than or less than 1, depending on the value of α (with equality obtained for $\alpha = 0.5$). This relationship illustrates the peculiarity of SEPIC converters with respect to the classical stepup or stepdown topologies. The more accurate expression A_a accounts for parasitic resistances in the circuit:

$A_a = [V_{out} + V_d + I_{out} (A_i R_{cp} + R_{L2})] / [V_{in} - A_i (R_{L1} + R_{sw}) I_{out} - R_{sw} I_{out}]$
(Eq. 3)

This formula lets you compute the minimum, typical and maximum amplification factors for V_{IN} (A_{amin}, A_{atyp}, and A_{amax}). The formula is recursive ("A" appears in both the result and the expression), but a few iterative calculations lead to the solution asymptotically. The expression neglects transition losses due to the switch Sw and reverse current in D1. Those losses are usually negligible, especially if Sw is a fast MOSFET and its drain-voltage excursion ($V_{IN} + V_{OUT} + V_D$) remains under 30V (the apparent limit for today's low-loss MOSFETs).

In some cases, you should also account for losses due to the reverse current of D1, and for core losses due to high-level induction gradients. You can extrapolate the corresponding values of α from Eq. 2:

α xxx = $A_{axxx} / (1+A_{axxx})$, where xxx is min, typ or max.
(Eq. 4)

The DC current through Cp is null, so the mean output current can only be supplied by L2:

$I_{OUT} = IL2$
(Eq. 5)

L2's power-dissipation requirement is eased, because the mean current into L2 always equals I_{OUT} and does not depend on variations of V_{IN}. To calculate the current into L1 (IL1), express the fact that no DC current can flow through Cp. Thus, the coulomb charge flowing during α T is perfectly balanced by an opposite coulomb charge during (1-α)T. When the switch is closed (for an interval α T) the node A potential is fixed at 0V. According to Equation 1, the node B potential is $-V_{IN}$, which reverse-biases D1. Current through Cp is then IL2. When the switch is open during (1-α)T, IL2 flows through D1 while IL1 flows through Cp: α T × IL2 = (1-α)T × IL1. Knowing that IL2 = I_{OUT},

$IL1 = A_{axxx} \times I_{OUT}$
(Eq. 6)

Because input power equals output power divided by efficiency, IL1 depends strongly on V_{IN}. For a given output power, IL1 increases if V_{IN} decreases. Knowing that IL2 (hence I_{OUT}) flows into Cp during α T, we choose Cp so that its ripple ΔV_{Cp} is a very small fraction of V_{Cp} (γ = 1% to 5%). The worst case occurs when V_{IN} is minimal.

$Cp \geq I_{OUT} \alpha_{min} T / (\gamma V_{INmin})$
(Eq. 7)

The combination of high-frequency controller operation and recent progress in multilayer ceramic

capacitors (MLCs) allows the use of small, non-polarized capacitors for Cp. Be sure that Cp is able to sustain the power dissipation Pcp due to its own internal resistance (Rcp):

$Pcp = A_{amin}\ Rcp\ I_{OUT}^2$
(Eq. 8)

Rsw, consisting usually of the MOSFET switch drain-to-source resistance in series with a shunt for limiting the maximum current, incurs the following loss:

$Psw = A_{amin}\ (1 + A_{amin})\ Rsw\ I_{OUT}^2$
(Eq. 9)

Losses Prl1 and Prl2 due to the internal resistances of L1 and L2 are easily calculated:

$Prl1 = A_{amin}^2\ Rl1\ I_{OUT}^2$
(Eq. 10)

$Prl2 = RL2\ I_{OUT}^2$
(Eq. 11)

When calculating the loss due to D1, take care to evaluate V_D for the sum of IL1 + IL2:

$PD1 = V_D \times I_{OUT}$
(Eq. 12)

L1 is chosen so its total current ripple (ΔIL1) is a fraction (β = 20% to 50%) of IL1. The worst case for β occurs when V_{IN} is maximum, because DIL1 is maximum when IL1 is minimum. Assuming β = 0.5:

$L1_{min} = 2\ T\ (1-\alpha_{max})\ V_{INmax} / I_{OUT}$
(Eq. 13)

Choose a standard value nearest to that calculated for L1, and make sure its saturation current meets the following condition:

$IL1_{sat} > > IL1 + 0.5\ \Delta IL1 = A_{amin}\ I_{OUT} + 0.5\ T\ \alpha_{min}\ V_{INmin} / L1$
(Eq. 14)

The calculation for L2 is similar to that for L1:

$L2_{min} = 2\ T\ \alpha_{max}\ V_{INmax}/I_{OUT}$
(Eq. 15)

$IL2_{sat} > > IL2 + 0.5\ \Delta IL2 = I_{OUT} + 0.5\ T\ \alpha_{max}\ V_{INmax} / L2$
(Eq. 16)

If L1 and L2 are wound on the same core, you must choose the larger of the two values. A single core compels the two windings to have the same number of turns and therefore the same inductance values. Otherwise, voltages across the two windings will differ and Cp will act as a short circuit to the difference. If the winding voltages are identical, they generate equal and cumulative current gradients. Thus, the natural inductance of each winding should equal only half of the value calculated for L1 and L2.

Because no great potential difference exists between the two windings, you can save costs by winding them together in the same operation. If the windings' cross sections are equivalent, the resistive losses will differ because their currents (IL1 and IL2) differ. Total loss, however, is lowest when losses are distributed equally between the two windings, so it is useful to set each winding's cross section according to the current it carries. This is particularly easy to do when the windings consist of splitted wire for counteracting skin effects. Finally, the core size is chosen to accommodate a saturation current much greater than (IL1 + IL2 + ΔIL1) at the highest core temperature anticipated.

The purpose of the output capacitor (C_{OUT}) is to average the current pulses supplied by D1 during Toff. The current transitions are brutal, so C_{OUT} should be a high-performance component like the one used in a flyback topology. Fortunately, today's ceramic capacitors provide low ESR. The minimum value for C_{OUT} is determined by the amount of ripple (ΔV_{OUT}) that can be tolerated:

$C_{OUT} > = A_{amin}\ I_{OUT}\ \alpha_{min}\ T / \Delta V_{OUT}$
(Eq. 17)

The value of an actual output capacitor may need to be much larger, especially if the load current is composed of high-energy pulses. The input capacitor can be very small, thanks to the filtering properties of the SEPIC topology. Usually, C_{IN} can be ten times smaller than C_{OUT}:

$C_{IN} = C_{OUT} / 10$
(Eq. 18)

Overall efficiency η can be predicted from V_{IN} and Aa. The result can be optimistic, however, because it doesn't account for the switch-transition losses or core losses:

$\eta = V_{OUT} / Aa\ V_{IN}$
(Eq. 19)

Finally, the switch SW and diode D1 should be rated for breakdown voltages respectively greater than V_{DS} and V_R:

$V_{DS} > 1.15\ (V_{OUT} + V_D + V_{IN})$
(Eq. 20)

$V_R > 1.15\ (V_{OUT} + V_{IN})$
(Eq. 21)

As an example, consider component ratings in the following low-power application: V_{INmin} = 2.7V, V_{INtyp} = 3.5V, and V_{INmax} = 5V, for V_{OUT} = 3.8V, I_{OUT} = 0.38A, T = 2µS, and V_D = 0.4V. A round of initial estimates gives the following approximate values: L1 and L2 = 47µH, RL1 = RL2 =120mΩ , Rcp = 50mΩ , and Rsw = 170mΩ . **Figure 3** shows the resulting IL1 and IL2 waveforms at different V_{IN} values.

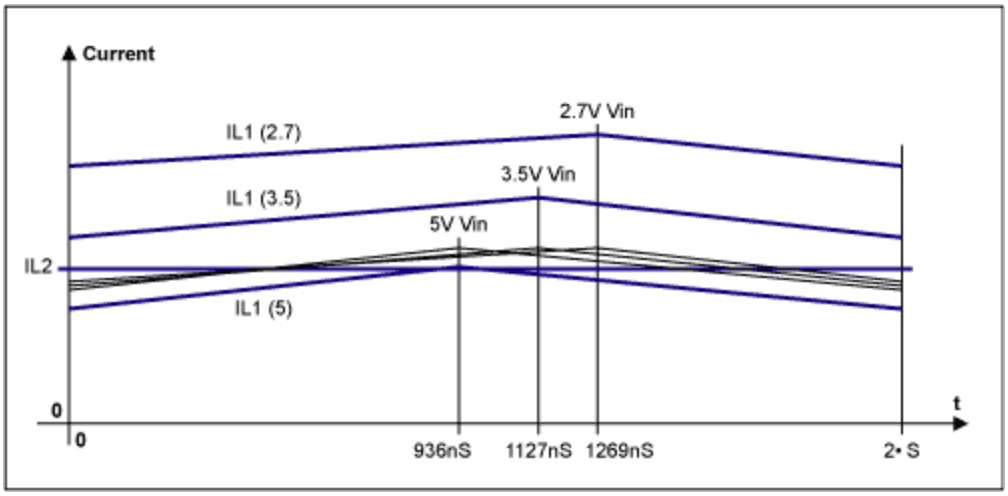

Figure 3. In Figure 2, the current waveforms through L1 and L2 vary with V_{IN} as shown.

Using Equation 2, you first calculate the ideal amplification factors Ai corresponding to minimum, typical, and maximum V_{IN} as 1.555, 1.2, and 0.84. Using these values in Equation 3, you obtain the more-accurate Aaxxx values of 1.735, 1.292, and 0.88 respectively. The corresponding duty cycles are deduced from Equation 4 as 0.634, 0.563, and 0.468.

The L2 current (IL2) equals 0.38A according to Equation 5, and IL1 varies according to V_{IN}. Using Equation 6, we obtain IL1 values of 0.659A, 0.491A and 0.334A as V_{IN} varies from minimum to maximum.

We obtain a minimum Cp value of 3.5µF by fixing γ = 5% in Equation 7. The voltage rating of Cp is deduced from Equation 1. If the input voltage is not to exceed 5V, a 6.8µF ceramic capacitor rated at 6.3V should do the job. Modern MLC capacitors easily meet the expected 50mΩ Rcp, and they easily sustain the 12.5mW power loss deduced from Equation 8.

The following parameters are computed at the worst case, which is minimal V_{IN}:

- A 170mΩ switch must dissipate 116.5mW according to Equation 9, which allows for the external transistor a SOT23 package or even the smaller SC70.
- Equations 10 and 11 give losses of 52.2mW and 17.3mW for L1 and L2. We verify here that the copper cross-section of L1 should be larger than that of L2.
- Using Equation 12 to calculate the power loss of D1 at 152mW, we see that D1 is the main source of loss. It is therefore important to choose an efficient rectifier, if not a synchronous rectifier.
- For L1, Equation 13 suggests a minimum value of 28µH, which is close to the estimated value of 47µH. For normal operation with an L1 value of 47µH, Equation 14 predicts a peak current of 0.69A. A device rated at 1A provides a reasonable margin. Make sure that D1 can sustain current pulses at high temperature equal to IL1 + I_{OUT} = 1.04A, and a mean current of I_{OUT} = 0.38A.
- Similarly, Equation 15 leads to a minimum L2 value of 24.6µH. Again, 47µH is a reasonable value. According to Equation 16, L2 should sustain current peaks of 0.43A.
- For ΔV_{OUT} (V_{OUT} / 100) of 38mV, Equation 17 says the output capacitor should be at least 22µF. Equation 18 says 2µF should be sufficient for C_{IN}.
- Despite high-valued parasitic components, Equation 19 predicts a respectable efficiency of 81% for the worst case, in which input voltage is minimum. When transition losses are taken into account, the actual value is a bit lower.

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