Application Note 3088

Writing and Reading Battery Management Devices

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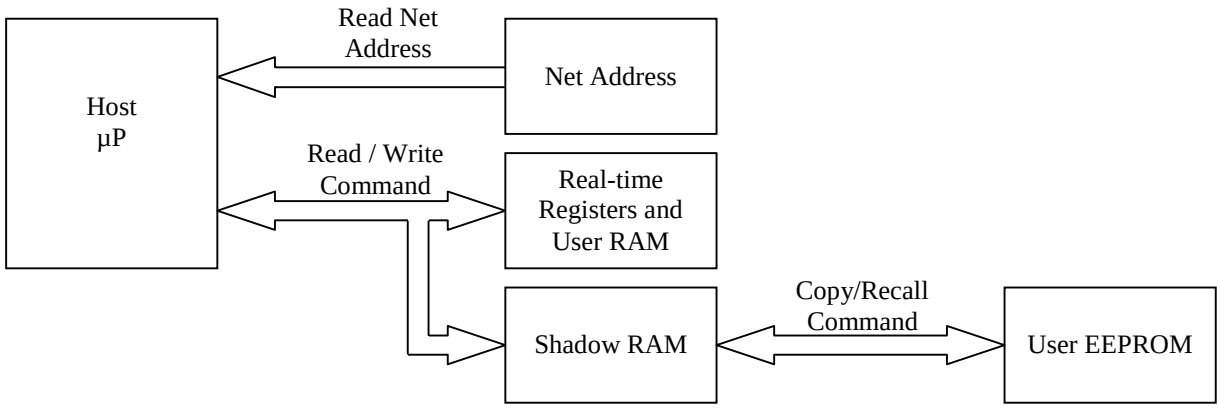
Introduction

Dallas Semiconductor Battery Management ICs share the same communication protocols and the same memory address locations for common functions. There are separate protocols for reading and writing each of the different types of memory available. This application note describes how to read the unique Net Address, write and read user RAM, and write and read EEPROM. These procedures apply to all battery management ICs. Timing diagrams are also included in the appendix.

Figure 1. Different Memory Types Inside a Battery Management IC



Reading the Net Address

The Read Net Address command (0x33h, selectable to 0x39h on some products) allows the bus master to read the unique address of the battery management device on the 1-Wire bus. The command is sent directly after a Reset/Presence Detect and is then followed by the 1-Wire slave transmitting its 64-bit address. See Figure 2 in the appendix for a timing diagram.

Table 1. Reading a Device's 64-Bit Unique Address

Operation	Hex Value	Transmitted by
RESET	N/A	MASTER
PRESENCE	N/A	SLAVE
READ NET ADDRESS	0x33h	MASTER
64 bit address	8 bytes	SLAVE

A Read Net Address command is valid if there is only one slave device on the 1-Wire bus. If there are more than one device or even the possibility of more than one device then a Search Net Address procedure must be used to determine the individual net addresses.

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Reading or Writing Real-Time Registers and User RAM

Register or RAM location access uses the format of a Reset / Presence Detect and a Net Address command followed by either the write or read command, the starting address, and then the data. If there is only one slave device on the bus a Skip Net Address can be used, otherwise the master must send a Match Net Address command followed by the 64-bit address of the device being communicated to before continuing with the sequence. Table 2 shows sample reads and writes of the ACR register. Note that the Read and Write commands as well as the address of the ACR register are the same for all battery management devices.

Table 2. Reading and Writing Registers or RAM in a Battery Management Device

Operation	Hex Value	Transmitted by
RESET	N/A	MASTER
PRESENCE	N/A	SLAVE
SKIP NET ADDRESS	0xCCh	MASTER
READ COMMAND	0x69h	MASTER
ACR ADDRESS	0x10h	MASTER
ACR MSB	1 byte	SLAVE
ACR LSB	1 byte	SLAVE
Operation	**Hex Value**	**Transmitted by**
RESET	N/A	MASTER
PRESENCE	N/A	SLAVE
SKIP NET ADDRESS	0xCCh	MASTER
WRITE COMMAND	0x6Ch	MASTER
ACR ADDRESS	0x10h	MASTER
ACR MSB	1 byte	MASTER
ACR LSB	1 byte	MASTER

The internal address pointer is incremented every time a byte is written or read, therefore the bus master can continue to read or write bytes through the end of the address space (0xFFh). Any location that is read only will not be overwritten and any location that is undefined will return unspecified data. See Figure 3 in the appendix for the timing diagram of a read operation.

Reading or Writing EEPROM Locations

EEPROM locations cannot be written to or read from directly. They are buffered with Shadow RAM. To write data to EEPROM, the data is first written to the Shadow RAM of the same address using a Write Command. The master then issues a Copy command and the slave device transfers the data from Shadow RAM into EEPROM. Similarly, a Recall command must first be issued to transfer the data from EEPROM into Shadow RAM before the master can read it.

Table 3. Reading a Block of EEPROM

Operation	Hex Value	Transmitted by
RESET	N/A	MASTER
PRESENCE	N/A	SLAVE
SKIP NET ADDRESS	0xCCh	MASTER
RECALL COMMAND	0xB8h	MASTER
BLOCK 0 ADDRESS	0x20h	MASTER
RESET	N/A	MASTER
PRESENCE	N/A	SLAVE
SKIP NET ADDRESS	0xCCh	MASTER
READ COMMAND	0x69h	MASTER
BLOCK 0 ADDRESS	0x20h	MASTER
Block 0 Data	16 bytes	SLAVE

Table 4. Writing an Entire Block of EEPROM

Operation	Hex Value	Transmitted by
RESET	N/A	MASTER
PRESENCE	N/A	SLAVE
WRITE COMMAND	0x6Ch	MASTER
BLOCK 0 ADDRESS	0x20h	MASTER
Data	16 bytes	MASTER
RESET	N/A	MASTER
PRESENCE	N/A	SLAVE
SKIP NET ADDRESS	0xCCh	MASTER
COPY COMMAND	0x48h	MASTER
BLOCK 0 ADDRESS	0x20h	MASTER

While reading and writing start at a specific address, Recall and Copy operations affect an entire block of memory at once. All 16 bytes are either recalled or copied. Therefore unless all 16 bytes are being written, it is important to recall the block before writing and copying the new data to prevent corruption of bytes not being updated as shown in Table 5. See Figures 4 and 5 in the appendix for timing diagrams of EEPROM reads and writes.

Table 5. Writing Only One Byte of EEPROM

Operation	Hex Value	Transmitted by
RESET	N/A	MASTER
PRESENCE	N/A	SLAVE
SKIP NET ADDRESS	0xCCh	MASTER
RECALL COMMAND	0xB8h	MASTER
BLOCK 0 ADDRESS	0x20h	MASTER
RESET	N/A	MASTER
PRESENCE	N/A	SLAVE
WRITE COMMAND	0x6Ch	MASTER
ADDRESS	0x25h	MASTER
Data	1 byte	MASTER
RESET	N/A	MASTER
PRESENCE	N/A	SLAVE
SKIP NET ADDRESS	0xCCh	MASTER
COPY COMMAND	0x48h	MASTER
BLOCK 0 ADDRESS	0x20h	MASTER

Summary

There are three different types of memory inside a battery management IC. The unique read-only 64-bit net address can be accessed through the Read Net Address command. All registers, user RAM, and EEPROM shadow RAM can be written to directly using Read and Write commands. EEPROM data cannot be written or read directly. The data must be passed through the Shadow RAM using a Copy or Recall command. The Copy and Recall commands operate on an entire block of memory at once so care must be taken not to accidentally overwrite other data located in the same memory block. These procedures for reading and writing data apply to all Dallas Semiconductor Battery Management devices.

Appendix

The following sample Figures show timing diagrams for different writing and reading operations for Battery Management ICs. See any 1-wire device datasheet for a description of the timing of individual bits.

Figure 2. Reading the Device Net Address

A read of the net address of any battery management device begins with the Read Net Address command followed by a read of 8 bytes starting with the family code byte and ending with the CRC byte.

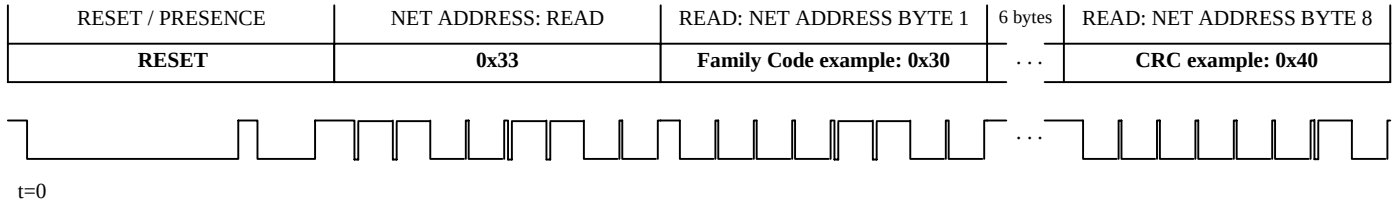

Figure 3. Reading the Real-Time Registers

This is a sample read from a DS2740. No recall command is needed because the real-time registers do not have shadow RAM. In this example the register contains the value 0x04E1 and the ACR contains the value 0xF480.

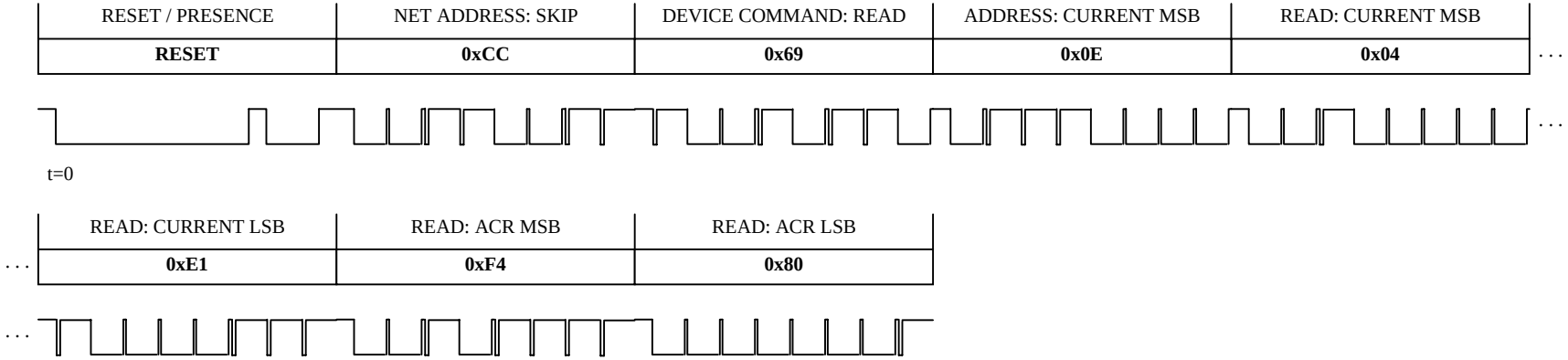

Figure 4. Reading EEPROM Bytes

This example reads the entire EEPROM block 0 inside a DS2762. A Recall command is called to update the shadow RAM before the read takes place.

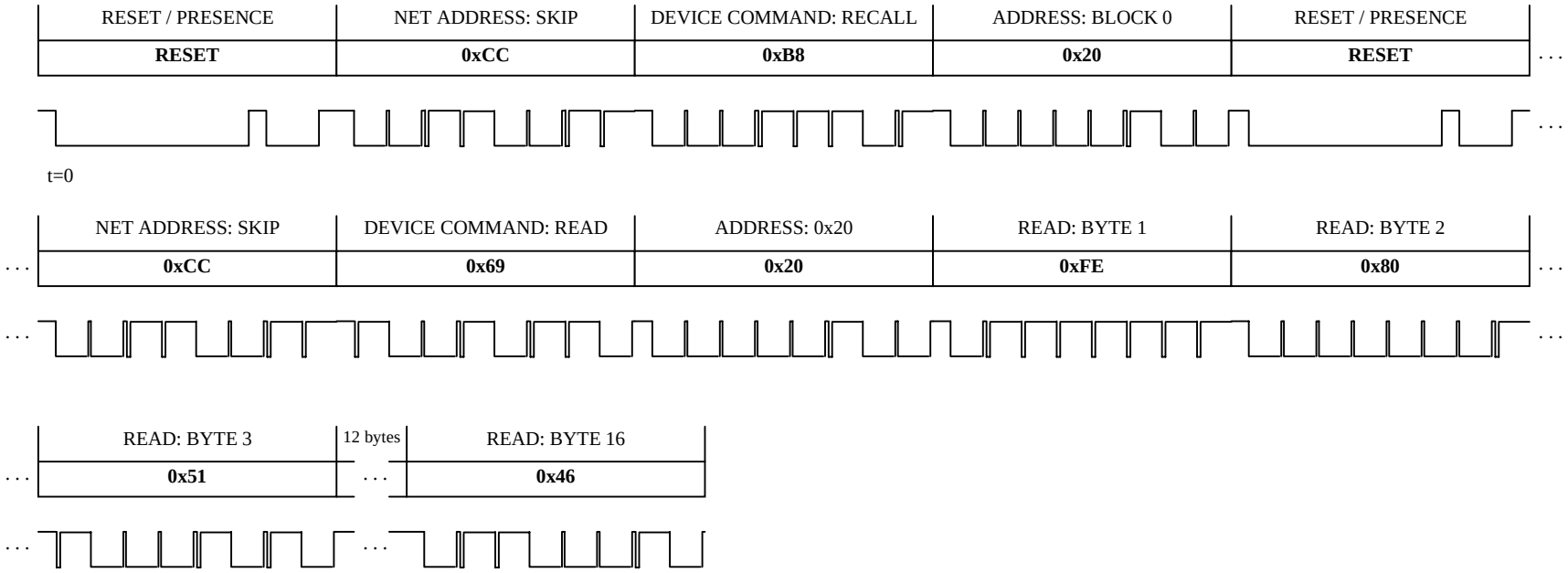

Figure 5. Writing EEPROM Bytes

This example writes 4 bytes of data to block 0 EEPROM inside a DS2762. A Recall command must first be sent so the other 12 bytes of data in block 0 are not disturbed by the write. Afterwards a Copy command is sent to transfer the data from shadow RAM to EEPROM.