Manufacturing with the 73M2901CE V.22 *bis* Single Chip Modem

The 73M2901CE integrated circuit modem provides all the microprocessor control and modulation and demodulation functions required to implement a V.22 *bis* 2400 bps modem. Standard practices require that a finished product must to meet a certain level of quality. In order to insure that level of quality, a manufacturer needs to include in the manufacturing process testing that will guarantee as much as possible the highest quality of its products.

This application note is intended to describe the tools contained in the 73M2901CE that can aid a manufacturer validating the manufacturing process and insure the high quality of the finished modem function. It will cover from the component level test to the functional test (usually performed for each finished product built) and up to the full QC monitoring test (performed on a significant volume of production). Obviously, those tests will have different requirements since the component level and functional test have to achieve as much coverage as possible while done in a minimum time whereas the full QC test allows for a full coverage and is less time critical.

Because the modem function is a combination of the modem device and the line interface, this application note tends to separate the two blocks, although there may be some overlap.

Content:
- Component level test

    The 73M2901CE
    The line interface
- Functional test

    The 73M2901CE
    The line interface

1 Component Level Test

The component level test is intended to insure that the positioning and soldering of a device has been performed properly. This test will not check the features of a device but rather will insure that it is correctly wired to any external component it needs to operate with (host processor, power supplies…) without any short or open circuits between pins. This test, due to its nature, has to be performed in combination with external resources such a host processor and/or power supplies, function generators etc. This is usually part of a component level test performed on every trace through test points included during the design and layout phase.

1.1 The 73M2901CE

The 73M2901CE is a 32-pin device.

Method	Pin/Signal Checked	Remarks	Number of Pin/Signal Checked
Host processor sends "**AT\<CR\>**" and checks the answer "OK"	VPD (3) VND (3) TxD RxD ASRCH(USR20)		9
Voltage measurements through test points	Vbg Vref	Voltage must be 1.19V\<V\<1.31V	2
Check oscillator signal	TxCLK RxCLK OSCIN OSCOUT	It is wise to check the frequency tolerance of the crystal through test points on the TXCLK pin. The modem must be transmitting for the clock to be seen at the TXCLK pin. RXCLK also is only available when in a connected state.	4
Host processor sends "**ATS72+4S101=82**" and checks through test points or port inputs that • **Relay=0** • **RI=1** • **DCD=0** • **DSR=1** • **CTS=0** • **USR11=1** • **USR10=0** Then sends "**ATS101=169**" and checks that • **Relay=1** • **RI=0** • **DCD=1** • **DSR=0** • **CTS=1** • **USR11=0** • **USR10=1**	$\overline{\text{Relay}}$ $\overline{\text{RI}}$ $\overline{\text{DCD}}$ $\overline{\text{DSR}}$ $\overline{\text{CTS}}$ USR11 USR10		7
Host sets RTS, sends a read request "**ATS101?\<CR\>**" and check that bit 2 is set then resets RTS, sends "**ATS101?\<CR\>**" and checks that bit 2 is reset.	RTS		1
Host sends "**AT@R\<CR\>**", sets $\overline{\text{RING}}$ and $\overline{\text{DTR}}$ and checks that $\overline{\text{RI}}$ and USR10 are set. Then host resets RING and DTR and checks that RI and USR10 are reset.	$\overline{\text{DTR}}$ $\overline{\text{RING}}$	This mode will loop the interrupt inputs to the user port pins. Needs a reset to exit.	2
Host performs a reset and checks that $\overline{\text{DSR}}$, $\overline{\text{DCD}}$ or $\overline{\text{CTS}}$ goes low (for 25ms within 250ms)	$\overline{\text{Reset}}$	There is no need to validate the timing.	1
Host sends "ATJ3\<CR\>". Check is performed by frequency check through test points.	VPA VNA TXAN TXAP		4
	RXA		1
	HBDEN		1
		Total	**32**

It has to be noted that these tests need to take into account the specific configuration of the design and can be slightly modified to be more effective. Some of these tests might be eliminated (therefore saving test time) depending on the functional test set up implemented.

1.2   The Line Interface

The line interface component level test is performed mostly through test points at the component level (proper value, proper orientation for diodes…). Functional test as discussed further on provides additional testing coverage.

2   Functional test

The functional test is intended to insure that the function considered is fully operational. In the case of a modem, special attention has to be taken since the whole function is always a combination of a modem device (the 73M2901CE) and a line interface.

The areas that need to be covered during a functional test are the ones that will allow the application/the user to operate satisfactorily as a modem, e.g.,

- Data transmission in the 73M2901CE
- Data reception in the 73M2901CE
- Carrier transmission over the line interface
- Carrier reception over the line interface
- Seizing of the line
- Pulse dial capability

The basic test set up is as following:
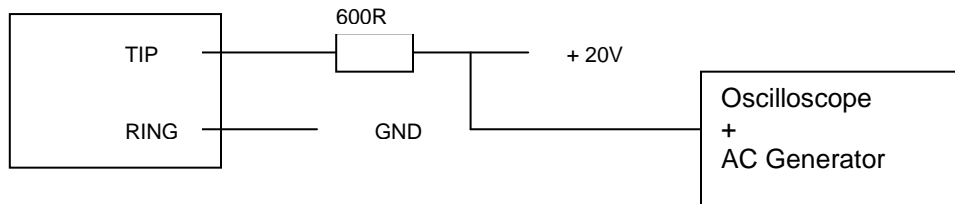
2.1   The 73M2901CE

Method	Function Checked	Remarks
Host processor sends "**ATS14+128@T1**", waits for the message "Connect…", sends a test pattern and checks the exact same pattern is returned. "+++AT@T0" to stop test.	Data transmission and reception in the low band	
Host processor sends "**ATS14-128@T1**", waits for the message "Connect…", sends a test pattern and checks the exact same pattern is returned. "+++AT@T0" to stop test.	Data transmission and reception in the high band	

This test activates all the internal circuitry of the 73M2901CE insuring a full coverage for data transmission and reception.

2.2   The Line Interface

Method	Function Checked	Remarks
Host sends "**ATH1**". Measure current through 600Ω resistor and check with reference.	Line seizing	
Host sends "**ATS101+2**". Measure current through 600Ω resistance and check with reference.	Pulse dialing	Test applicable if pulse dialing is controlled through Relay and Pulse signal.
Host sends "**ATJ2**" and oscilloscope checks for presence of 2100Hz energy on 600Ω resistor.	Carrier transmission over the line interface	This test needs only to insure that an AC signal can pass over the line interface
AC function generator sends a 2100Hz AC signal. Host sends "ATJ6" and "ATS62?" and checks that bit 2 is set (2100Hz detected).	Carrier reception over the line interface	This test needs only to insure that an AC signal can pass over the line interface

Revision History

Revision	Date	Description
1.2	7/07/2004	First publication.
2.0	11/12/2008	Converted original version 1.2 to Teridian format, removed all references to TDK and changed the document number from AN-2901-004 to AN_2901CE-028. There is no change to technical content.

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