
Measuring crosstalk penalty in high-speed bidirectional serial communication modules

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1 Introduction

Electromagnetic crosstalk poses a serious problem within today's advanced serial communication modules. A major detrimental effect is the degradation of receiver sensitivity in the presence of crosstalk noise. The mitigation of crosstalk penalty becomes increasingly more challenging as data rates increase for higher throughput, as module sizes shrink for increased port density, and as supply rails are reduced for lower power dissipation.

In this article, we explore a method for quantifying crosstalk penalty by observing a receiver's bit-error-ratio (BER) versus the phase difference between the transmitted and received signals. This article also presents actual crosstalk measurement results of three different communication module examples.

2 Background

2.1 Defining crosstalk

The crosstalk between two channels is defined as the ratio of the output of channel A (with no input signal) divided by the output of channel B (excited by input signal).

The crosstalk in dB from B to A is defined as

$$\text{Crosstalk} = 20 \log \frac{|V_{OA}|}{|V_{OB}|} \text{ dB} \quad (1)$$

and would ideally be negative infinity in dB for isolated channels¹. For bidirectional modules, channel A would represent the output of the receiver pre-amplifier and channel B would be the output of the transmitter driver, as depicted in Figure 1.

2.2 Defining crosstalk penalty

For the purpose of this article, crosstalk penalty is defined as receiver sensitivity degradation due to electromagnetic susceptibility to conducted and/or emitted transmitter radiation. High-speed circuits make heavy use of dynamic circuits, which are particularly sensitive to noise at their inputs². Two types of crosstalk-induced errors, temporal and logic, exist. Temporal errors refer to delay aberrations due to crosstalk, and logic errors result from improper evaluation in dynamic circuits³. In this article we focus on crosstalk-induced logic errors, which designers quantify using the BER (bit-error ratio) of the received signal.

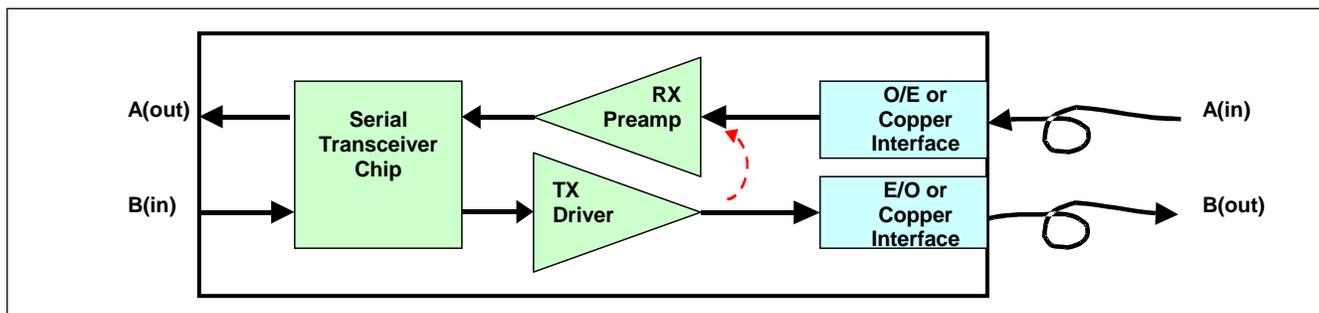


Figure 1. Simplified bidirectional communication module, depicting crosstalk from transmitter (Channel B) to receiver (Channel A).

3 Quantifying crosstalk

3.1 Direct measurement

Direct measurement of crosstalk can be a daunting task. Circuit topologies, impedance levels, physical layout, and IC technology all play critical roles in crosstalk strength. Differential circuit topology is gaining popularity due to its increased crosstalk immunity and increased dynamic range over ground-referenced (single-ended) circuits. However, due to a lack of accurate differential measurement capability, crosstalk between two complex circuits may be difficult or even impossible to measure, simulate or predict.

One method that overcomes this difficulty is direct measurement with a PMVNA (pure-mode vector network analyzer), which measures the differential-mode and common-mode responses of a device in terms of mixed-mode scattering parameters. Accurately capturing mixed-mode S-parameters enables direct measurement of the RF crosstalk between differential circuits, even in cases in which the crosstalk exceeds the modeling capabilities of electromagnetic simulators. Interested readers can find more details in an article by Bockelman and Eisenstadt⁴. Although effective, this method requires expensive equipment and direct access to the circuits under test.

To amplify the visible effects of crosstalk, we can employ three methods as described in a popular book by Howard Johnson⁵: turning off the primary (monitored) signal, turning off the crosstalk source, or by generating artificial crosstalk. Turning off the primary signal can be accomplished by short-circuiting its driver to ground with a very short, low inductance connection. Short circuiting is critical, since noise coupled through mutual inductance will disappear if the driver is left open-circuited. Crosstalk should stand out clearly with the output driver turned off. The crosstalk source can be disabled either by cutting the interfering line or by short-circuiting the aggressor driver; in either case, current must be reduced to zero. With the primary driver enabled, you can observe before-and-after waveforms; on digital scopes with math capability, the waveforms can be aligned and subtracted to get the differential. Artificial crosstalk can be induced by replacing the aggressor driver with a step function of known rise time, and crosstalk will be proportional to the induced dv/dt on the victim net.

This procedure is a test you should use before populating the pc board with components, so that you can isolate and identify crosstalk sources.

These experiments require either disassembly or partial destruction of the device under test, which can completely alter the environment surrounding the crosstalk conditions. Although these methods provide a means of identifying crosstalk sources, they do not provide what we really need to know about crosstalk – its relative performance penalty.

3.2 A better way: BER measurement

We can see from the preceding section that direct measurement of crosstalk in assembled modules is difficult to accomplish, which leads us to look for a better method. Good news—there *is* a better way. Using equipment that would usually be found in a well-equipped communication module development lab, we can perform indirect measurement of crosstalk by measuring what really counts: the sensitivity penalty imposed on the receive data path due to crosstalk from the transmit data path. Let's now find out how to perform indirect crosstalk quantification through measurement of the receiver BER penalty.

4 Example crosstalk penalty measurements

The three real-life measurement examples that follow represent a cross-section of high-speed communication modules that are available today: a 2.5Gbps fiber optic transceiver, a 10Gbps serial transceiver chip and a 10Gbps fiber optic transponder. Although these examples do not cover every application, they may serve as a basis for measurement methods that can easily be applied to other modules.

A similar approach is taken for each example. For modules operating strictly in the electrical domain, testing requires a precision reference clock, a serial line-rate pattern generator, an electrical attenuator, a variable phase delay element, a CDR (clock-and-data-recovery) unit, and a serial BERT (bit-error-rate tester). At line rates of 2.5Gbps and beyond, it is likely that the modules contain optics. This necessitates additional hardware: an optical transmitter, optical attenuator and optical power meter. Let's now get into the measurements.

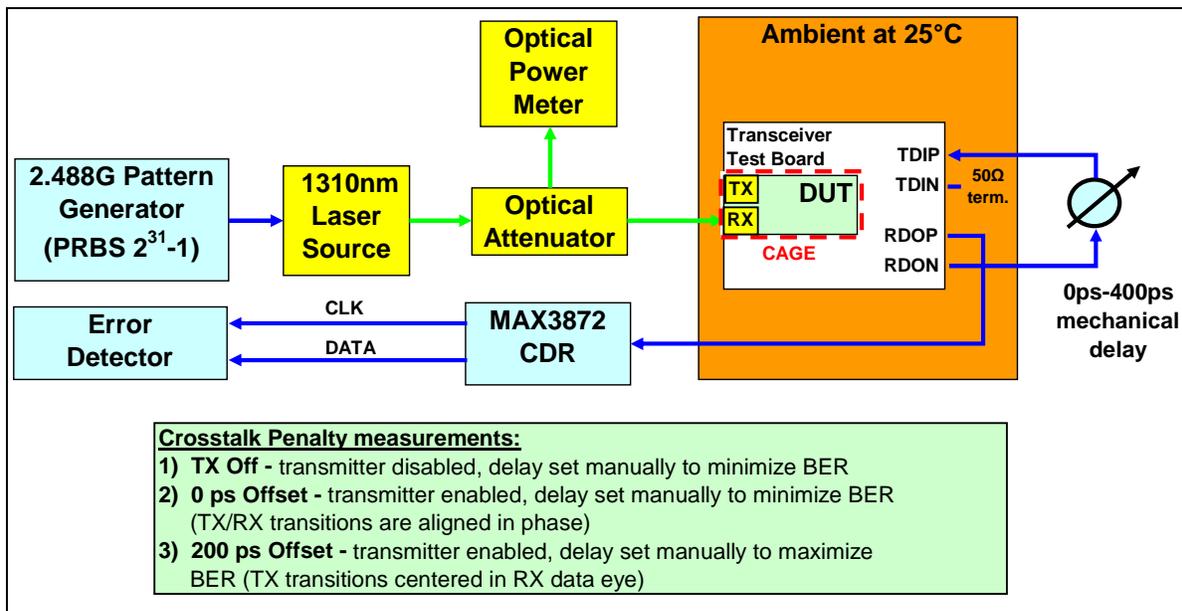


Figure 2. Setup diagram for testing crosstalk penalty of a 2.5Gbps serial fiber optic transceiver.

4.1 2.5Gbps serial fiber optic transceiver

An MSA (multisource agreement), under which several manufacturers collaborate to guarantee interchangeability and interoperability, specifies the form and function of the 2.5Gbps fiber-optic serial transceiver. With a few line rate and CDR modifications, the test setup depicted in Figure 2 could be used to test transceivers covered by this MSA from 155Mbps to 4.25Gbps.

The DUT (device-under-test) is a pluggable device that is inserted in a cage on a test board. In this example, the input to the device's optical receiver is a 1310nm laser transmitter driven by a 2.488Gbps pattern generator. The pattern is PRBS (pseudo-random binary sequence) with a seed of $2^{31}-1$, which creates a signal with a wide range of frequencies. The laser source is fed to an adjustable optical attenuator with a power tap to measure the optical power to the DUT. The receiver path of the transceiver contains an APD (avalanche photodiode) to create an output current proportional to incident optical power, a TIA (transimpedance amplifier) to convert the current to an analog voltage, and a limiting amplifier to create a digital output from the analog voltage. The output is differential, in which the non-inverting signal is sent to a CDR unit which derives clock and data for the error detector.

Here's the important part: the inverting output is fed to a variable phase delay element, which is essentially a coaxial tube (trombone) with a rotary dial that serves as a mechanical line stretcher. The variably delayed signal then routes to the input of the transceiver's transmitter. The phase relationship between transmitting signal and receiving signal can then be adjusted to maximize or minimize the crosstalk penalty, as seen by the relative difference in BER at the error detector.

Measuring the sensitivity of the transceiver's receiver involves adjusting the optical attenuation in 0.5dB increments and measuring the resulting BER. For this example, sensitivity is determined as the input level where $BER = 1e-10$, or one error per 10 billion bits. To measure the sensitivity penalty induced by crosstalk from the transmitter, three sensitivity curves were measured as shown and described in Figure 3. The best sensitivity of $-31dBm$ was measured when the transmitter was completely disabled. The best-case crosstalk penalty of 0.3dB was experienced when the transmitter transitions were phase-aligned with the receiver transitions. The worst-case penalty of 1.3dB was measured when the transmitter transitions were in the center of the received data eye, which is 200-psec offset for a 2.5Gbps signal (400-psec bit period). We see from these measurements that the phase relationship between the transmitted signal and received signal is a significant factor in determining the worst-case crosstalk penalty.

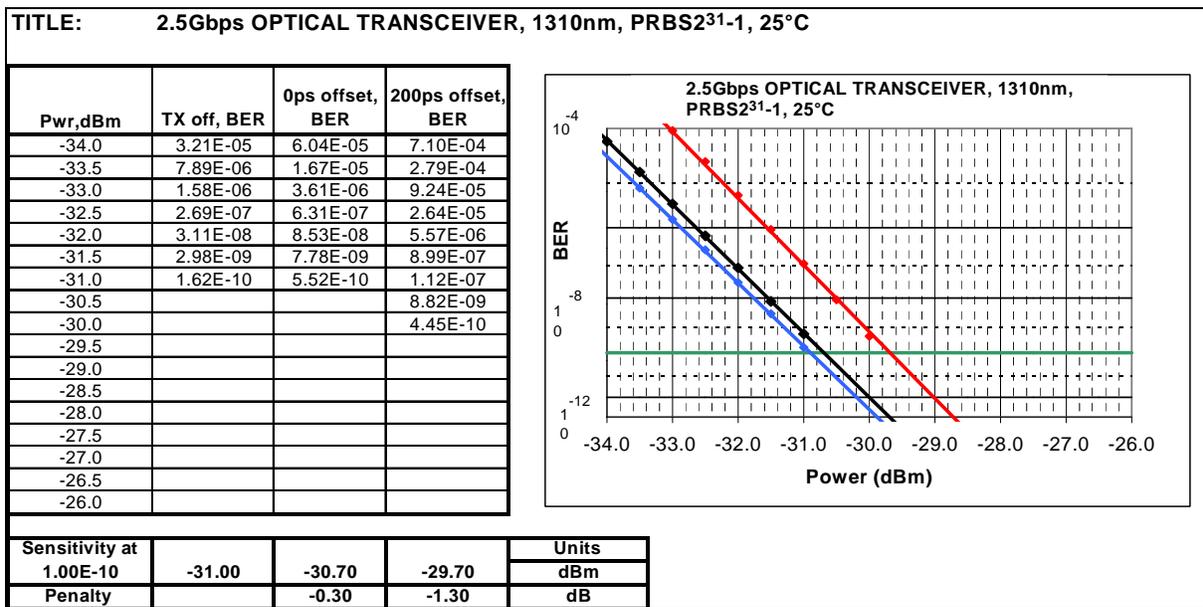


Figure 3. Sensitivity penalty measurement of a 2.5Gbps, 40km serial optical transceiver with a) transmit data disabled b) transmit data enabled with transitions phase-aligned with the receive data and c) transmit data enabled with 0.5 UI (400-psec) phase offset from the receive data.

4.2 10Gbps serial transceiver IC

The next example measures the crosstalk penalty of a 10Gbps, bidirectional serial-transceiver chip with CDR functions in each direction for data retiming (Figure 4). A chip of this type finds use in copper or fiber-optic transceivers, at serial line rates of 9.95- to 11.1Gbps - for example, within XFP (10 Gigabit

Small Form Factor Pluggable Module) MSA-compliant modules. We can see the setup diagram for testing the crosstalk penalty for this type of IC in Figure 4. The testing of these devices is less complex than that of the fiber optic transceiver, since they can be tested entirely in the electrical domain.

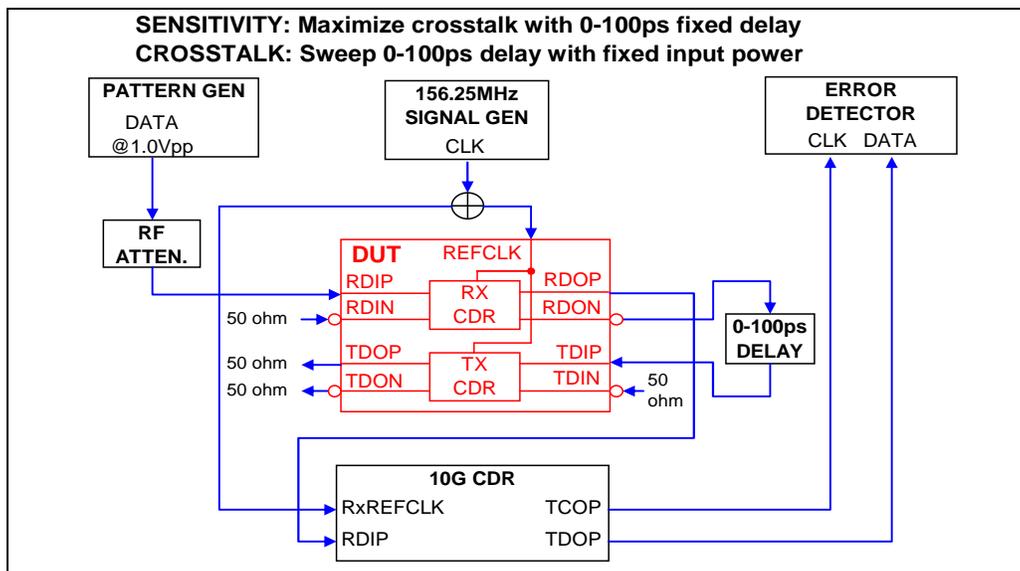


Figure 4. Setup diagram for testing crosstalk penalty of a 10Gbps bidirectional serial transceiver with dual clock and data recovery (CDR) circuits.

A manually adjusted, electrically attenuated serial PRBS data stream is generated from a pattern generator, which is routed into the receiver path input of the device under test. One half of the differential receiver output is fed to an external CDR, which performs clock and data recovery to drive the error detector. The other half of the differential receiver output is fed to a manual delay element and back into the transmitter path input. The transmitter is terminated with 50 ohm loads to stress the driver, and the transmitter to receiver signal delay is swept from 0 to 100-psec, or one UI (one unit interval at 10Gbps).

The crosstalk penalty is the BER variation of the received signal over the 0 to 100-psec delay sweep while the input was attenuated to keep the receiver in an errored state - approximately $1e-6$ BER. Although this BER range is not useful in real applications, we can see in Figure 5 that it provides a good picture of the phase-related BER variation. This particular device experienced approximately two decades of swing in the BER at a nominal BER of $1e-7$, or 1 error per 10Mb.

We can also quantify the crosstalk by the sensitivity difference at the minimum BER (with transmitter transitions aligned with the receiver transitions)

versus the maximum BER (with transmitter transitions in the center of the received data eye). For this example, sensitivity is determined as the input level where $BER = 1e-12$, or one error per trillion bits.

We see the corresponding sensitivity penalty in Figure 6, which in this case was 1.2dB in the electrical-voltage domain. With the transmitter disabled, this device had a measured receiver input sensitivity of 13.5mV differential. At the worst-case phase difference between transmit and receive signals (0.5 UI, or 50-psec), the sensitivity degrades to 15.5mV differential. This decreased sensitivity may at first glance seem insignificant, but if this device were assembled in an optical transceiver, an adverse impact on system performance might be the result. The optical power sensitivity penalty would be exactly one half of the electrical voltage sensitivity penalty, or 0.6dB; the optical link power budget would decrease by this amount. Another detrimental effect would be the premature and artificial trip of a LOS (loss-of-signal), if the host module contained one, when the input signal was near the comparison threshold.

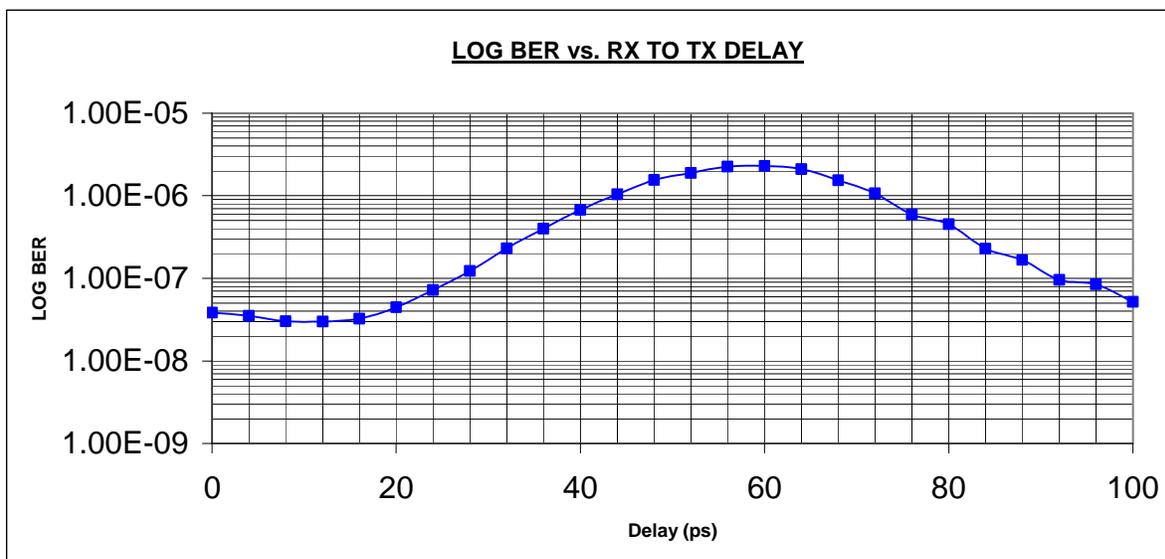
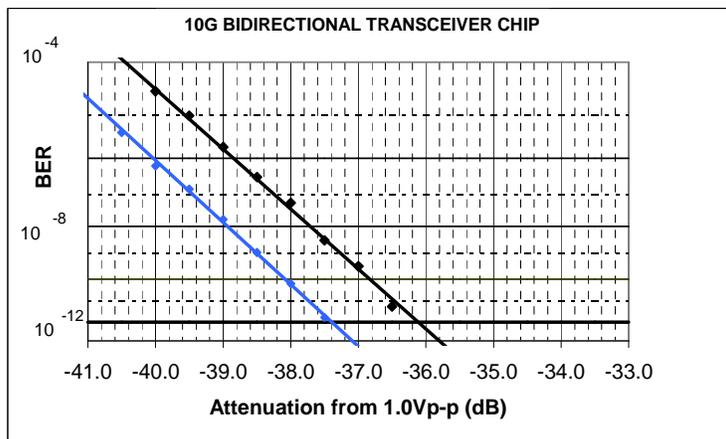


Figure 5. Sensitivity variation of the receiver as transmitted signal to received signal delay is varied by one UI (100-psec). Device under test is a 10G bidirectional serial transceiver chip with dual CDR circuits.

TITLE: 10G BIDIRECTIONAL TRANSCEIVER CHIP

Att, dB	TX OFF	MAX CROSSTALK
-41.0	2.58E-05	3.13E-04
-40.5	4.16E-06	1.02E-04
-40.0	6.29E-07	3.01E-05
-39.5	1.44E-07	9.69E-06
-39.0	1.68E-08	1.89E-06
-38.5	1.16E-09	3.17E-07
-38.0	6.24E-11	5.67E-08
-37.5	1.71E-12	3.21E-09
-37.0		3.31E-10
-36.5		5.85E-12
-36.0		
-35.5		
-35.0		
-34.5		
-34.0		
-33.5		
-33.0		



Sensitivity @ 1e-12		Penalty
dB	-37.40	-36.20
mV	13.50	15.49
dBm	-23.01	-22.41

Optical estimate; assumes 3K transimpedance gain, 0.9 photodiode responsivity

Figure 6. Sensitivity measurement of the receiver of a bidirectional serial transceiver chip with a) TX data disabled and b) TX data enabled with 0.5 UI (50-psec) phase offset from the received data.

4.3 10Gbps fiber optic transponder

Our last and most complex example involves the crosstalk penalty measurement of a 300-pin, 622Mbps parallel to 10Gbps serial fiber optic transponder. We see the block diagram of the test setup in Figure 7. Although these devices are not fully serial, they contain a serial transmitter and

receiver pair for transmission over optical fiber. The transmitter and receiver optical engines respectively mate with a 16:1 multiplexer and a 1:16 demultiplexer. The setup is similar to that of the 2.5Gbps transceiver with some notable exceptions: the line rate is at 10Gbps, the data on the electrical module interface is parallel at 1/16 the speed of the line rate and reference clocks are required for data recovery and retiming.

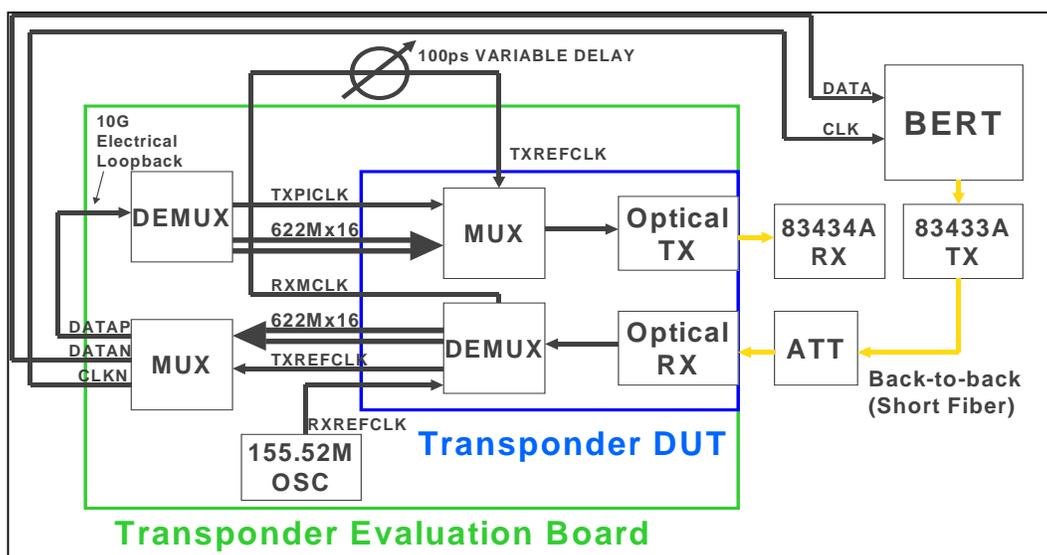


Figure 7. Setup diagram for testing crosstalk penalty of a 622Mbps parallel to 10Gbps serial multiplexing/demultiplexing fiber optic transponder.

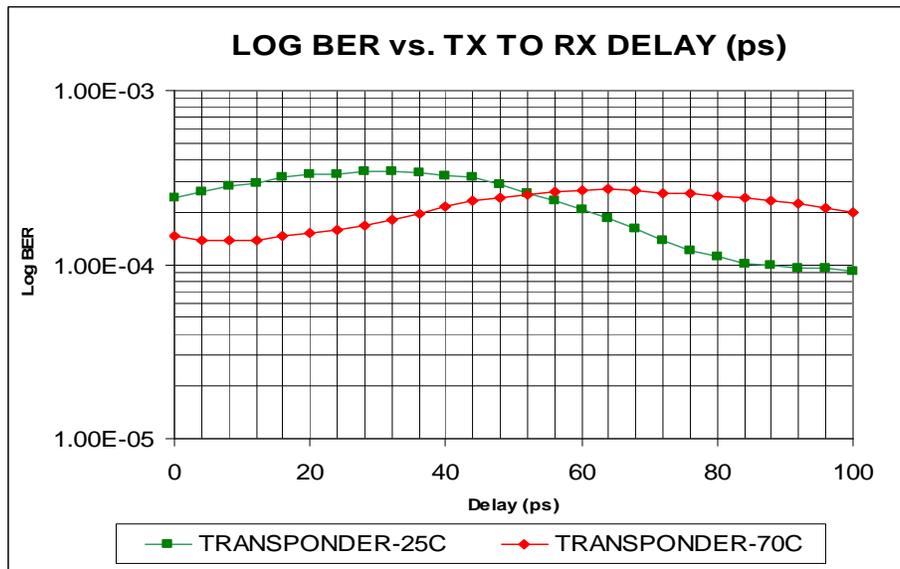


Figure 8. Bit error ratio variation of a 300-pin, 622Mbps-parallel to 10Gbps-serial multiplexing/demultiplexing fiber optic transponder as the transmitter to receiver data delay is varied by one unit interval (100ps), measured at 25°C and 70°C.

The data originates from a PRBS $2^{31}-1$ pattern generator signal at 9.95328Gbps (OC-192 SONET rate), driving a lab-standard 1550-nm laser transmitter. The optical data then goes to an optical attenuator with a calibrated power tap for monitoring the input level to the transponder under test. The receiver path of the transponder uses a reference clock to perform clock and data recovery; it then demultiplexes the serial data into 16 parallel channels. The parallel data electrically loops back with a parallel data clock to the transmitter-path multiplexer, through an external multiplexer/demultiplexer pair on the transponder evaluation board. The reference clock for the transmitter, which retimes the data for serial transmission, is a delayed copy of the receive path recovered clock; a data FIFO enables the transmitter parallel clock and serial clock to be different. The phase relationship of the serial transmitter data to the serial receiver data can then be manually adjusted for the crosstalk measurement. The BERT is driven directly from an external 16:1 multiplexer in the receiver path, allowing the BER of the receiver to be measured independent of the transmitter path while the receiver is experiencing crosstalk from the transmitter.

We see the resulting BER variation as the serial transmitter data delay is swept from 0 to 100-psec in relation to the serial receiver data in Figure 8. The measurement was taken at both 25°C and an elevated

temperature of 70°C with similar results. The BER variation is approximately one half decade at an error ratio of $1e-4$ (1 error per 10kb). This BER variation translates to approximately 0.3dB sensitivity penalty in the optical domain.

5 Conclusion

Crosstalk in bidirectional serial communication modules is a complex and elusive phenomenon that is not easily quantified. We have learned that direct measurement of crosstalk in the time domain or frequency domain is not always feasible within a module, and removal of the housing would change the environmental conditions. This led us to explore a new crosstalk measurement method, allowing the module to be tested as a complete entity in its native operating condition. This provides an accurate and realistic measurement of the maximum crosstalk penalty that would be expected in a real application, the performance parameter that really counts.

Crosstalk is inevitable within any enclosure with bidirectional transmission, but if we employ good RF design practice the penalty experienced by crosstalk noise can be substantially reduced. As technology advances enable smaller and faster electronic devices, we must place more emphasis on designing for crosstalk isolation to maintain the high level of signal integrity that future advanced communication systems will require.

6 Recommended Maxim components

155Mbps-4.25Gbps serial transceiver

MAX1932	Digitally Controlled, 0.5% Accurate, Safest APD Bias Supply
MAX3658	622Mbps, Low-Noise, High-Gain Transimpedance Preamplifier
MAX3744, MAX3745	2.7Gbps SFP Transimpedance Amplifiers with RSSI
MAX3738	155Mbps to 4.25Gbps SFF/SFP Laser Driver with Extinction Ratio Control
MAX3799	1Gbps to 14Gbps, SFP+ Multirate Limiting Amplifier and VCSEL Driver
MAX3748A	Compact 155Mbps to 4.25Gbps Limiting Amplifier
MAX3735A	2.7Gbps, Low-Power SFP Laser Driver
MAX3740A	3.2Gbps SFP VCSEL Driver with Diagnostic Monitors
MAX3795	1Gbps to 4.25Gbps Multirate VCSEL Driver with Diagnostic Monitors
MAX3982	1Gbps to 4.25Gbps SFP Copper Cable Pre-emphasis Driver
DS1864	SFP Laser Controller and Diagnostic IC
MAX4007, MAX4008	High-Accuracy, 76V, High-Side Current Monitors in SOT23
MAX15059	76V, 300mW Boost Converter and Current Monitor for APD Bias Applications

9.95Gbps-10.7Gbps fiber optic transponder, serial transceiver

MAX3945	1.0625Gbps to 11.3Gbps, SFP+ Dual-Path Limiting Amplifier
MAX3941	10Gbps, 3Vp-p EAM Driver with Integrated Bias Network
MAX3942	10Gbps, 6Vp-p Modulator Driver
MAX3946	1.0625Gbps to 11.3Gbps, SFP+ Laser Driver with Laser Impedance Mismatch Tolerance
MAX3799	1Gbps to 14Gbps, SFP+ Multirate Limiting Amplifier and VCSEL Driver
MAX3984	1Gbps to 10Gbps Pre-emphasis Driver with Receive Equalizer
MAX3991, MAX3992	10Gbps CDR with Limiting Amplifier and 10Gbps CDR with Equalizer
MAX3622	Low-Jitter, Precision Clock Generator with Two Outputs
MAX8520, MAX8521	Smallest TEC Power Drivers for Optical Modules
DS1862A	XFP Laser Control & Digital Diagnostics IC
DS1874	SFP+ Controller with Digital LDD Interface

Maxim offers an extensive product portfolio of analog and mixed-signal components for virtually any electrical design application.

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² A. Vittal, L.H. Chen, M. Marek-Sadowska, K. Wang, and S. Yang, “Crosstalk in VLSI Interconnections”. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 18, No. 12, pp. 1817-24, December 1999.

³ H. Chou, and S. Chiu, “Crosstalk Reduction and Tolerance in Deep Sub-Micron Interconnects”. Department of Electrical and Computer Engineering, University of Wisconsin, Madison, WI.

⁴ D.E. Bockelman and W.R. Eisenstadt, “Direct Measurement of Crosstalk Between Integrated Differential Circuits”, *IEEE Transactions on Microwave Theory and Techniques*, Vol. 48, No. 8, August 2000, pp. 1410-13.

⁵ H. Johnson and M. Graham, *High-Speed Digital Design: A Handbook of Black Magic*. Prentice Hall PTR: Upper Saddle River, NJ, 1993, pp. 189-211.